COMP 506, Spring 2019
Practice Final Exam

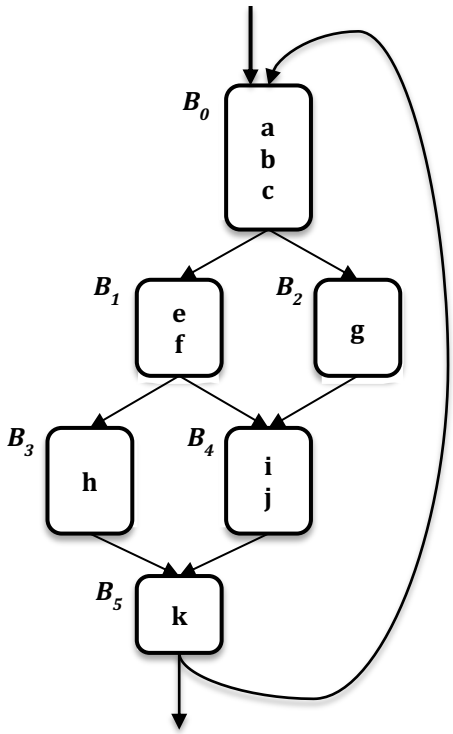
1. **Compare And Contrast:**
   Define each term in two or three sentences. Explain the difference between the two terms. Your answer cannot be longer than one page.
   a. Loop unrolling (Lec 21) versus loop-invariant code motion (Lec 20)
   b. Minimal SSA form and Semi-pruned SSA Form
   c. Value numbering (Lec 16) versus global redundancy elimination (Lec 19)
   d. Local scheduling (Lec 26) versus trace scheduling (Lec 27)

2. **Short Answer Questions:**
   a. In local value numbering, how can the compiler check to see if an operation can be simplified due to an algebraic identity? How can the compiler writer make sure that the cost of that check stays constant and bounded?
   b. In global redundancy elimination using ***available expressions***, the domain (or name space of the problem) is the set of all expressions in the program. That domain can grow quite large. How might you shrink that name space without hurting the effectiveness of the optimization? (Hint: think semi-pruned.)
   c. In list scheduling, the algorithm maintains a set of operations that are ready to be scheduled, often called the ***ready list***. Some authors advocate using a priority queue to implement the ready list. Others advocate a simple set representation. Discuss the tradeoff between these two different implementations.

3. **System Knowledge**
   a. Modern computer systems typically have multi-level cache memories. What is the difference between a shared cache and a private cache?
   b. If a computer has a direct-mapped level 1 data cache with 512 lines, each of which contains 64 bytes of data, what is the total capacity of the level 1 data cache.
   c. If a computer has a 4-way, set-associative level 1 data cache with 256 sets and cache lines of 64 bytes, what is the total capacity of the level 1 data cache?
   d. To manage the cache, a processor typically breaks the address into three fields: a tag, an index, and an offset. Assume that you are designing a new model of an existing processor and that the index field is fixed at s bits and the offset field is fixed at o bits. (The cache has 2^s sets; lines contain 2^o bytes.) What cache parameters can you change, other than s and o to let your processor address a larger level one cache?

4. Optimization and Graph Manipulations

Compiler writers must be comfortable manipulating and using graphs.



a. How many extended basic blocks are in the control-flow graph to the right? Which basic blocks are in each extended basic block?

b. Compute a postorder traversal and a reverse postorder traversal for the example graph

c. Draw that graph that would result from applying superblock cloning to the example graph.

d. If you converted the code for this graph into static single-assignment form (**SSA** form), which nodes might contain phi-functions?