Adaptive Noise Cancellation using the LMS Algorithm

December 7, 1999
Functional Description

• Adaptive Noise Cancellation DSP Circuit
  - Removes background noise from signals
• Application: Pilot Communication
  - Two signals:
    • Noise + Pilot’s Speech
    • Noise Reference Signal in Cockpit
Functional Description (cont’d)

- Filter input $x(k)$ to obtain $y(k)$
- Error $e(k) = \text{Desired Input } d(k) - y(k)$
  - Used to update filter frequency response
- 8-tap Finite Impulse Response (FIR) Filter
- LMS Algorithm
  - $W(k+1) = W(k) + u \times 2 e(k) \times x(k)$
  - Fixed Step-Size $u$
Overview

- Circuit Design
- PLA Description
- Layout
- System Performance Analysis
System Block Diagram

A Booth Recoding Multiplier
8bit x 8bit

Multiplier P[0,3]  
Adder A[0,1] B[0,1]  
Multiplier A[0,1] B[0,1]  
PLA state bits [0,3]  

DEBUG BLOCK
System Timing: Error Calculation
System Timing: Weight Update
Circuit Design

- 12-bit Carry-Look Ahead Adder
- 8-bit Radix-4 Booth Recoding Multiplier
- 8-bit Rotate Stack
Carry-Look Ahead Adder

4-bit Carry Look-Ahead Adder
Radix-4 Booth Recoding Multiplier
Rotate Stack
PLA Description

• 15 states, 5 inputs, 17 outputs

• 2 Phases:
  - Error Computation
  - Filter Tap Weight Update

• 2 Counters (count to 8):
  - Counter to count multiplier clock cycles
  - Counter to count # of multiply operations

• One Iteration ~200 clock cycles
State Diagram
-- Elec 422 Project MAIN CONTROLLER PLA

INPUTS:  RESTART COUNT8 COUNT9;

OUTPUTS:  STOREXD STOREW ROTATEX ROTATEW MDS MWE
           MMULT LOADMULT CLRCNT8 CLRCNT9 CNT8A CNT8B
           SUBTRACT LACCUM LERROR CLRALL CLRACCUM;

-- reset logic
reset on RESTART to init(CLRA   ALL CLRACCUM);

init:  -- initial state --> clear all latches
    goto LoadXD(STOREXD LOADMULT CLRCNT8 CLRCNT9);

LoadXD:   -- X & D inputs
    goto RotateXW(ROTATEX ROTATEW CNT8A);

RotateXW:    -- rotate X & W stacks
    goto StartCNT8b(CNT8B);

StartCNT8b:   -- signal 8 counter w/ second control signal
    goto WaitMultXWDone;

WaitMultXWDone: -- wait for the multiply of X & W to finish
    case (COUNT9 COUNT8)
        10 => StartNextMultXW(LOADMULT LACCUM CLRCNT9);
        11 => StartNextMultXW(LACCUM);
    endcase => WaitMultXWDone;

StartNextMultXW:  
    if COUNT8 then CalculateE(MMULT SUBTRACT)  
        else RotateXW(ROTATEX ROTATEW CNT8A);

CalculateE:  
    goto GetE(MMULT SUBTRACT LERROR);

GetE:  
    goto WaitBeforeMult;  -- CLKB2 happens on EVEN cycles

WaitBeforeMult:  
    goto StartMultXE(MWE LOADMULT CLRCNT8 CLRCNT9
                        CLRACCUM);

StartMultXE:  
    goto GetWAdd(ROTATEX ROTATEW MDS MMULT CNT8A);

GetWAdd:  
    goto StartCNT8b2(MDS MMULT CNT8B LACCUM);

StartCNT8b2:  
    goto WaitMultXEDone(MDS);

WaitMultXEDone: -- wait for the multiply of X & W to finish
    case (COUNT9 COUNT8)
        10 => StartNextMultXE(MDS MWE STOREW LOADMULT
                                   CLRCNT9);
        11 => StartNextMultXE(MDS STOREW ROTATEX);
    endcase => WaitMultXEDone(MDS);

StartNextMultXE:  
    if COUNT8 then WaitBeforeMult2  -- CLKB2 happens on EVEN
                        cycles
        else StartMultXE(CLRA   ALL);

WaitBeforeMult2:  
    goto init(CLRA   ALL CLRACCUM);
Layout

- Cell Hierarchy
- Plots of Low-Level Cells
- Floorplan
- Full plot of Chip
Cell Hierarchy

- PLA
  - Counter
  - 8-bit Multiplier
    - Product Register
    - Clearable Latch
  - 8-bit Adder
  - 4-bit Adder
- Full Chip
  - 12-bit Adder/Accumulator
  - 4-bit Adder
  - 4-bit Adder
- Leaf Cells

- 8-bit Stack
- 2x12-bit MUX
- 2x8-bit MUX
- 8-bit Latch
- 8-bit Latch

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XOR Gate Cell
5-Input NAND Gate Cell
Static Latch
Clearable Static Latch
4-bit Carry-Look Ahead Adder
12-bit Carry-Look Ahead Adder
8-bit Radix-4 Booth Recoding Mult.
8x8-bit Rotate Stack
Control PLA & Counters
Floorplan
Full Plot of Chip

- 5,600T Total
System Performance Analysis

- Longest Path: Multiplier Output to Error Output Latch
  - 12-bit Adder in critical path

- Spice Analysis of 12-bit Adder
Spice Analysis (Rise Time)

- Rise Time \(\sim 23.5\) ns

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Spice Analysis (Fall Time)

- Fall Time \(~22\) ns
Summary of System Performance

- 12-bit Adder Worst Case Delay: ~25 ns
- Maximum Clock Speed: ~42.6 MHz