



Elec 423
April 26, 2000

Adaptive Noise Cancellation using the LMS Algorithm (NOISE KILA)

Wednesday April 26, 2000

GROUP Y

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Overview



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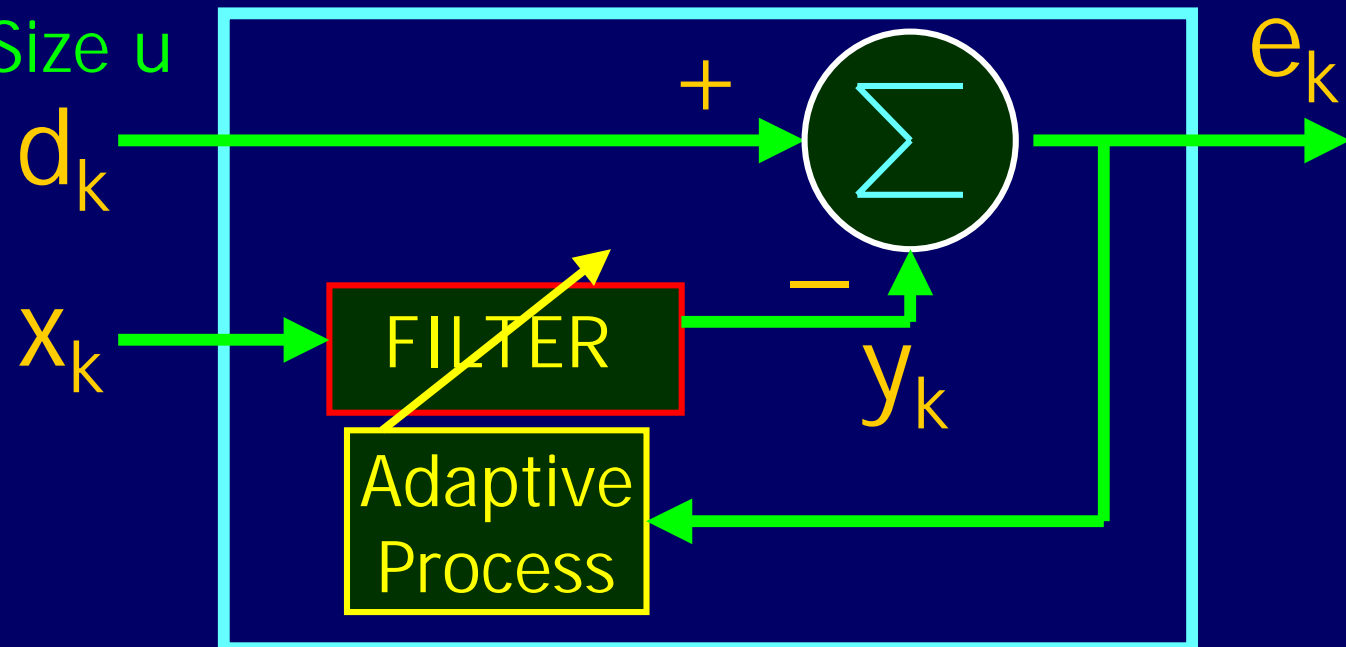
- Functional Description
- Debugging Features of our Chip
- Test Results
- Speed Test Results
- Yield

Functional Description



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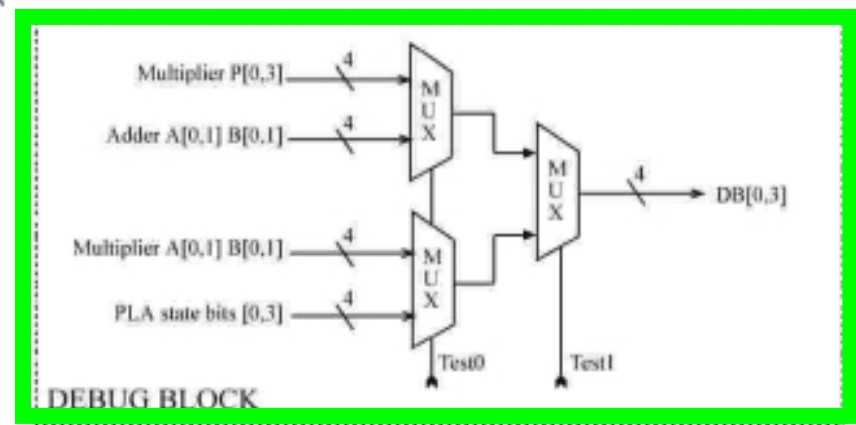
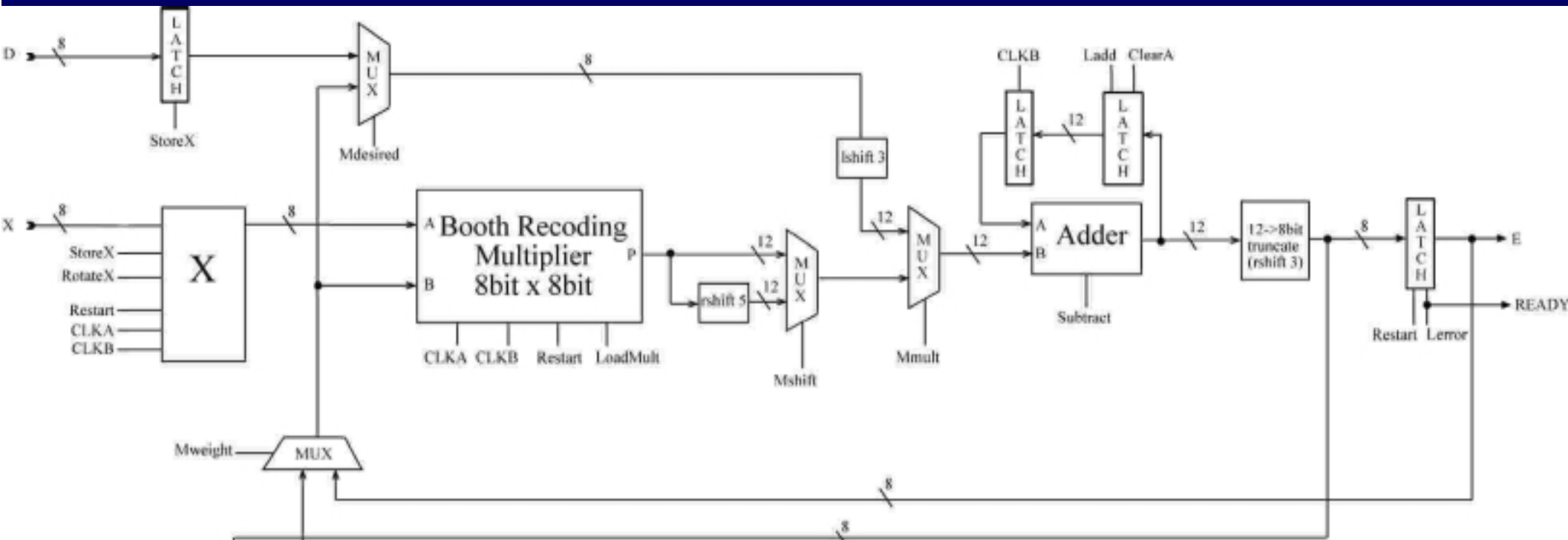
- Filter input $x(k)$ to obtain $y(k)$
- Error $e(k) = \text{Desired Input } d(k) - y(k)$
 - Used to update filter frequency response
- 8-tap Finite Impulse Response (FIR) Filter
- LMS Algorithm
 - $W(k+1) = W(k) + u * 2e(k) * x(k)$
 - Fixed Step-Size u



Debugging Features of Our Chip



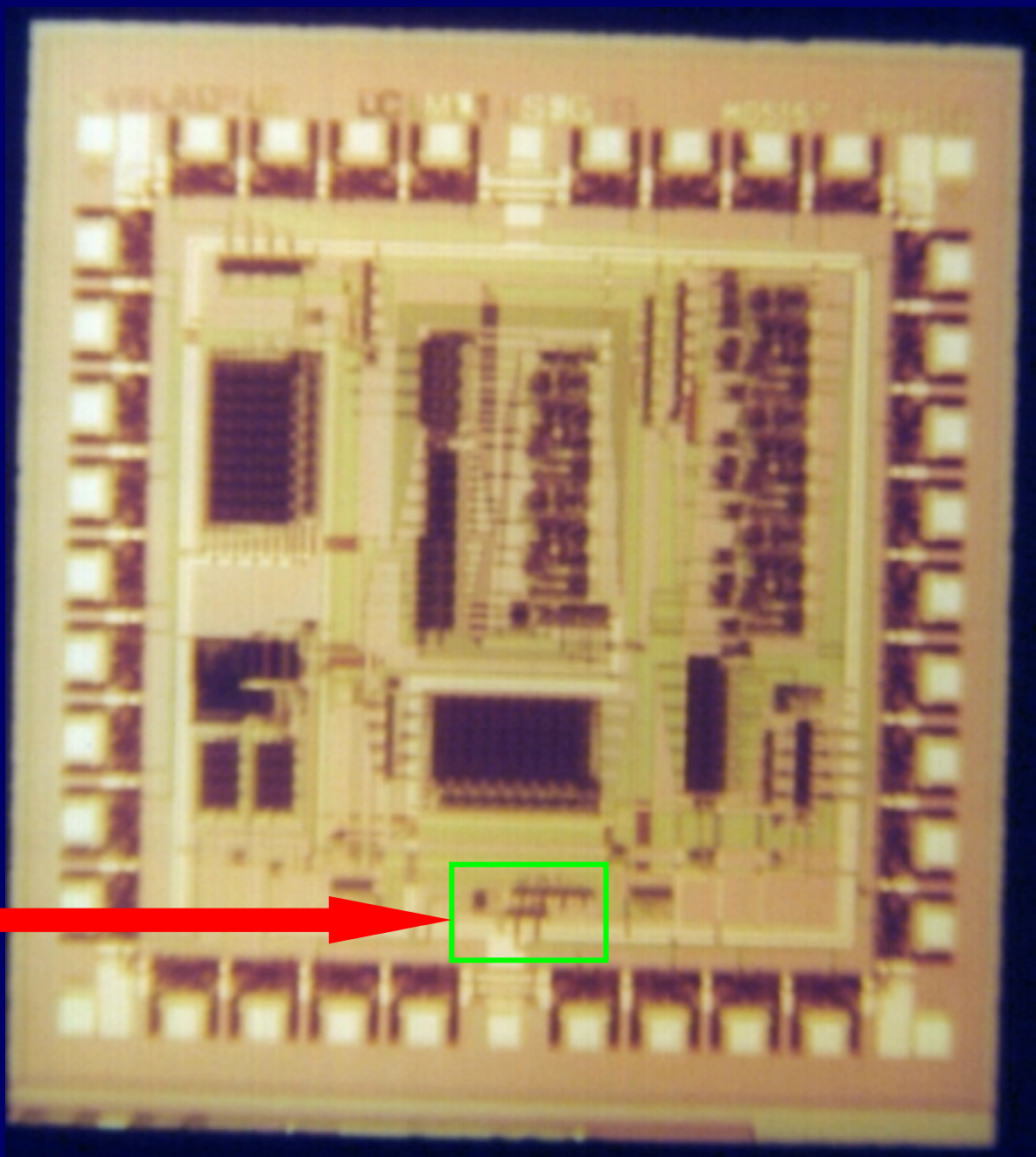
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Picture of Chip



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Debug Outputs



Test Results



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- Simple Testing Runs
 - Noise Cancellator Prototype

Limitation w/ OmniLab Testing



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- Only able to debug a MAX of 5 iterations
 - OmniLab has 4096 bit buffer per stimulation
 - Chip needs 175 clock cycles x 4 (2-phase clock)
 - $4096 / 700 = 5$ iterations

Simple Testing Run



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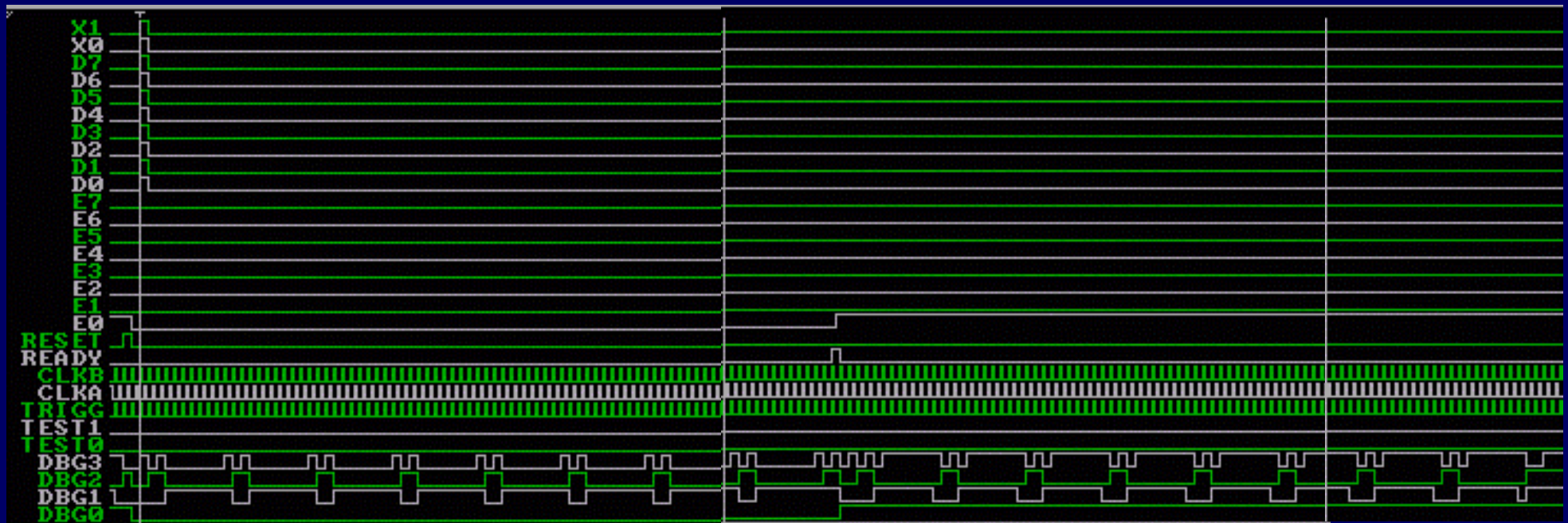
- 4 Test Vectors (sequentially) for Verification of Functionality
- Used DEBUG outputs to check for internal functionality (4 Different Outputs)
 - State Machine State Bits (4 bits)
 - Multiplier Inputs A (bits 0, 1) and B (bits 0, 1)
 - Multiplier Product Output (bits 0 – 3)
 - Adder Inputs A (bits 0, 1) and B (bits 0, 1)

State Machine Bits



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- Chip successfully traverses all states (approx. 180 clock cycles)
 - First Half – Error Calculation
 - Second Half – Filter Tap Weights Update

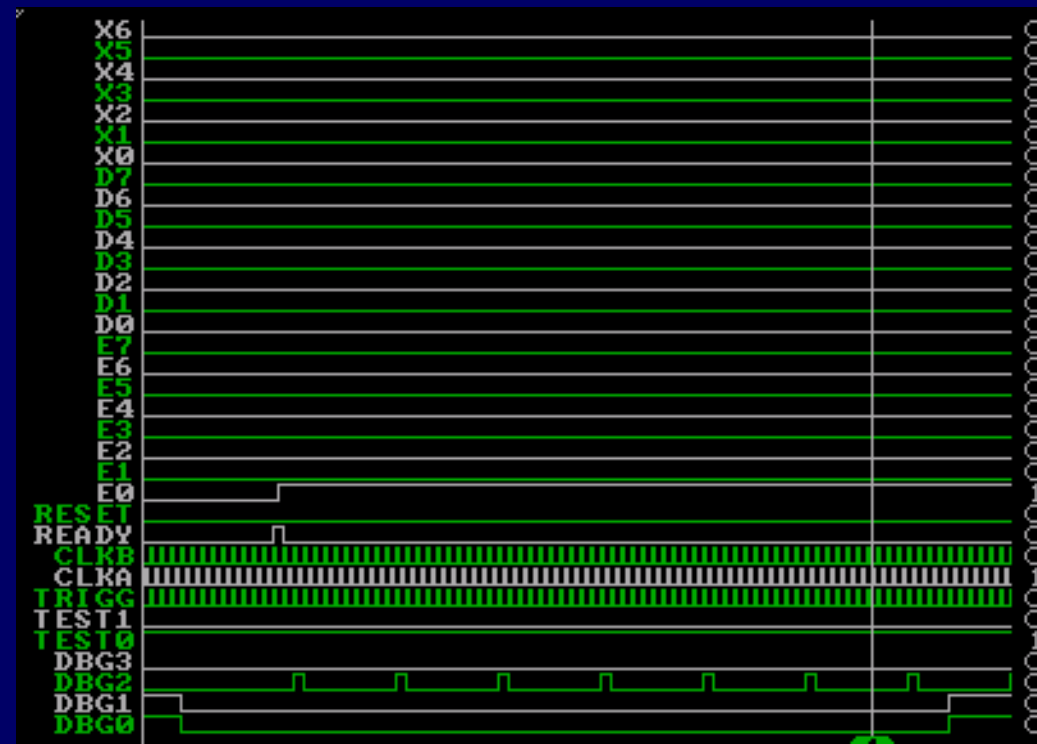
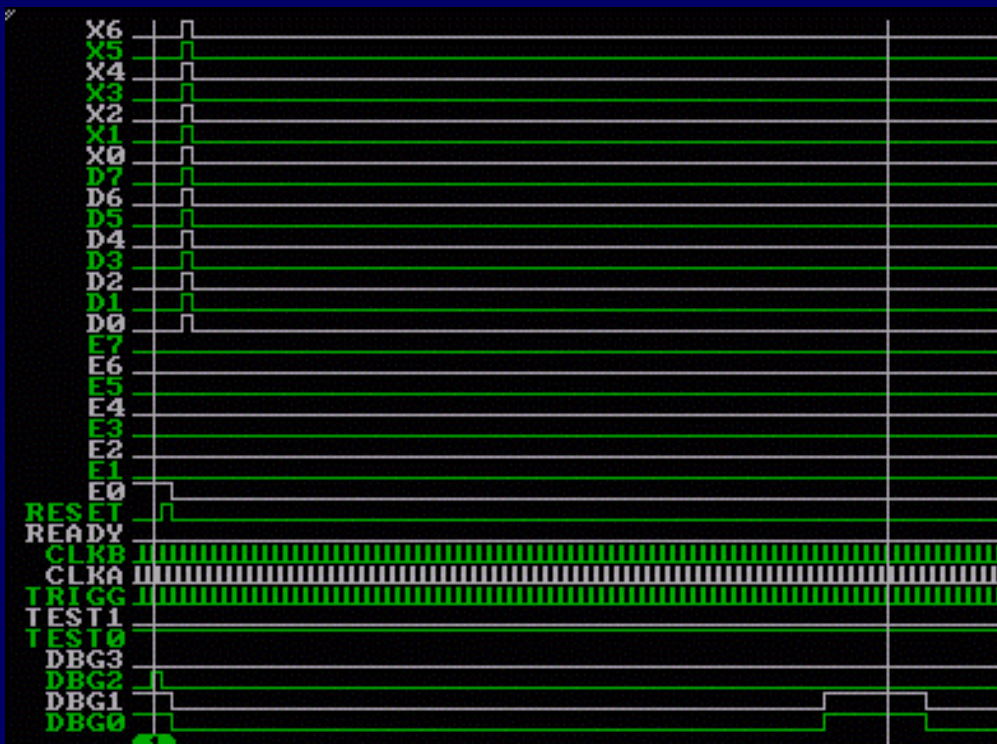


First Input in Simple Test



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- Both X and D are FFh
- Since the Filter Weights are initially 0, the Error Output is $(0 - (-1)) \Rightarrow 1$
- Verified Multiplier Inputs A (0, 1) and B (0, 1)

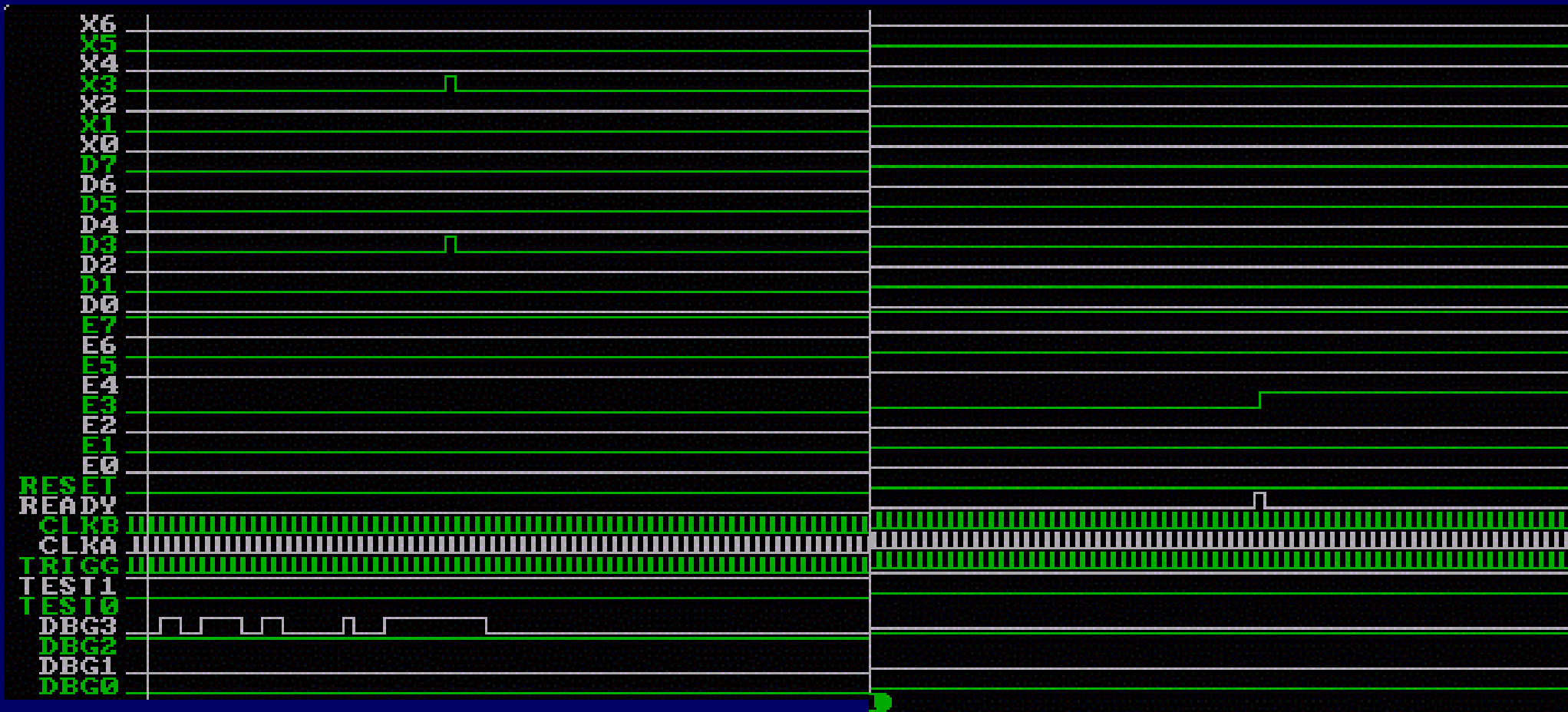


Last Input in Simple Test



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- X is 08h and D is 08h
- Error Output is F8h



Noise Canceller Prototype



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- Two A/D converters used for converting X and D inputs
- One A/D converter for output signal
- Initially we were not using the A/D & D/A converters correctly so not sure of correctness yet

Speed Test Results



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- Works up to maximum frequency in OmniLab (34 MHz / 4)
- Works using Functional Generator at 36MHz

Yield



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- 4 out of 5 chips work
 - Fifth chip was plugged in upside down
 - Unable to determine whether it was fabricated without error