

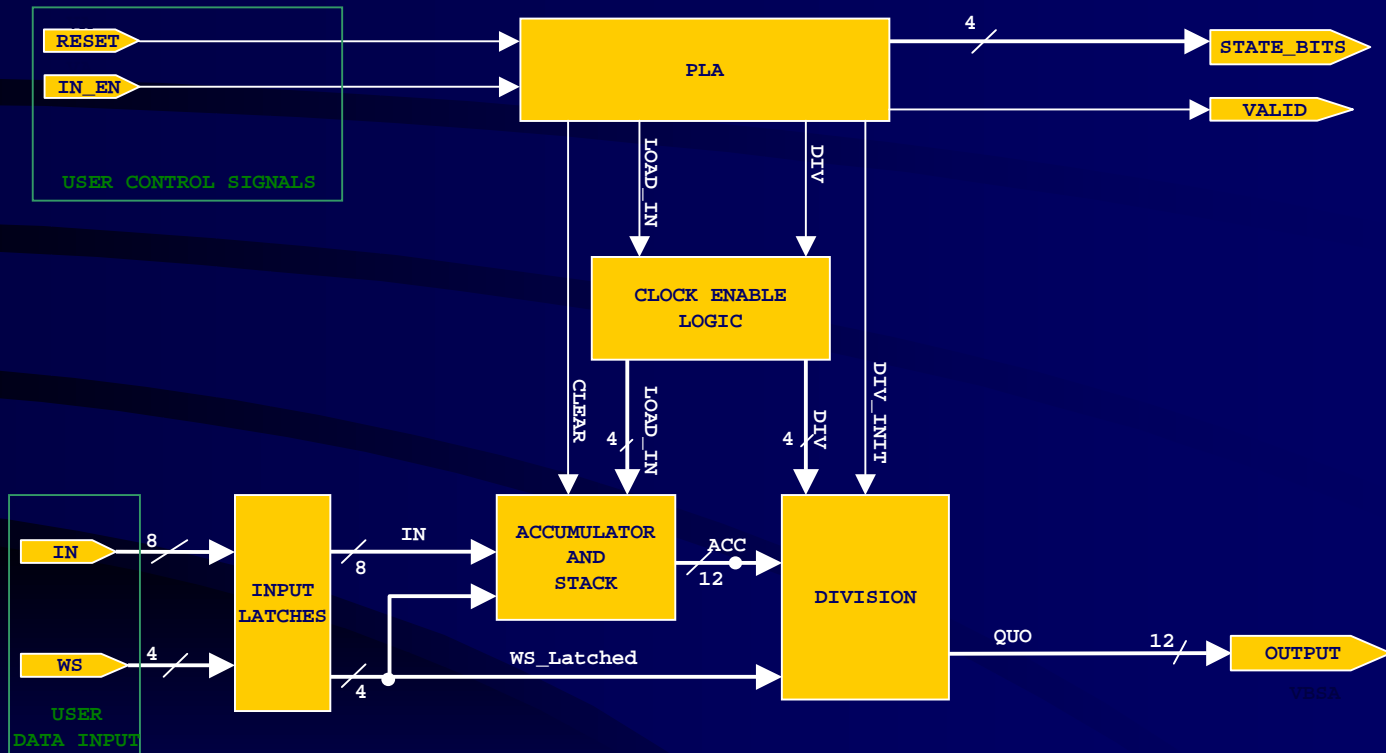
Averaging Serial-Input Circuit (ASIC)

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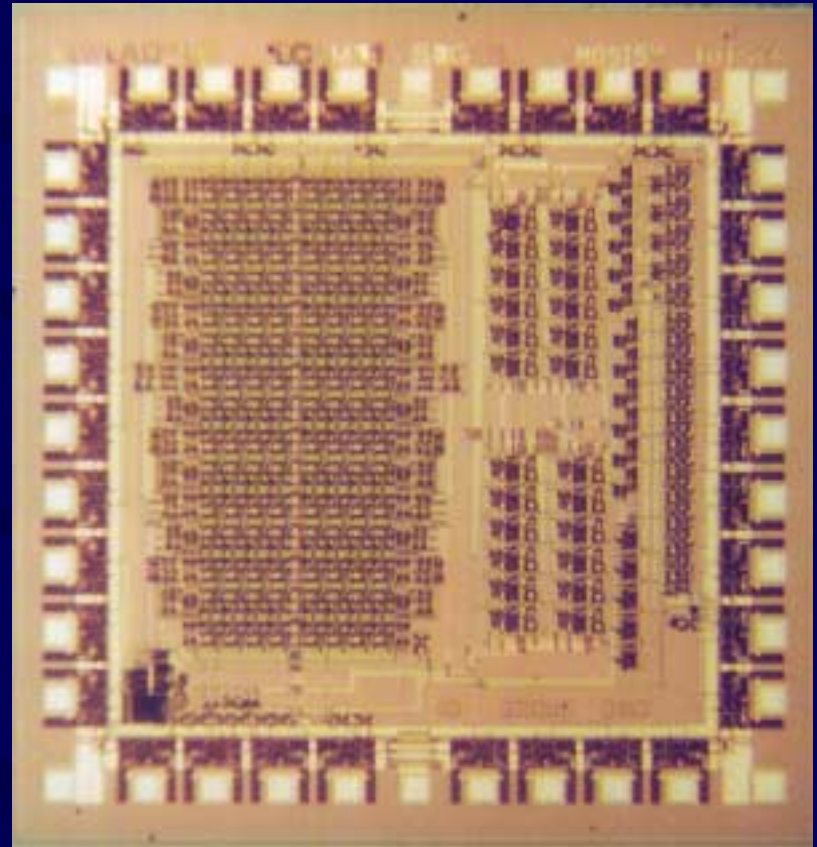
Jacky Chang

ASIC Functional Diagram



ASIC

- Design contains approximately 6000 transistors
- Stack with multiplexer (the monstrosity on the left) took up roughly 44% of the available chip area

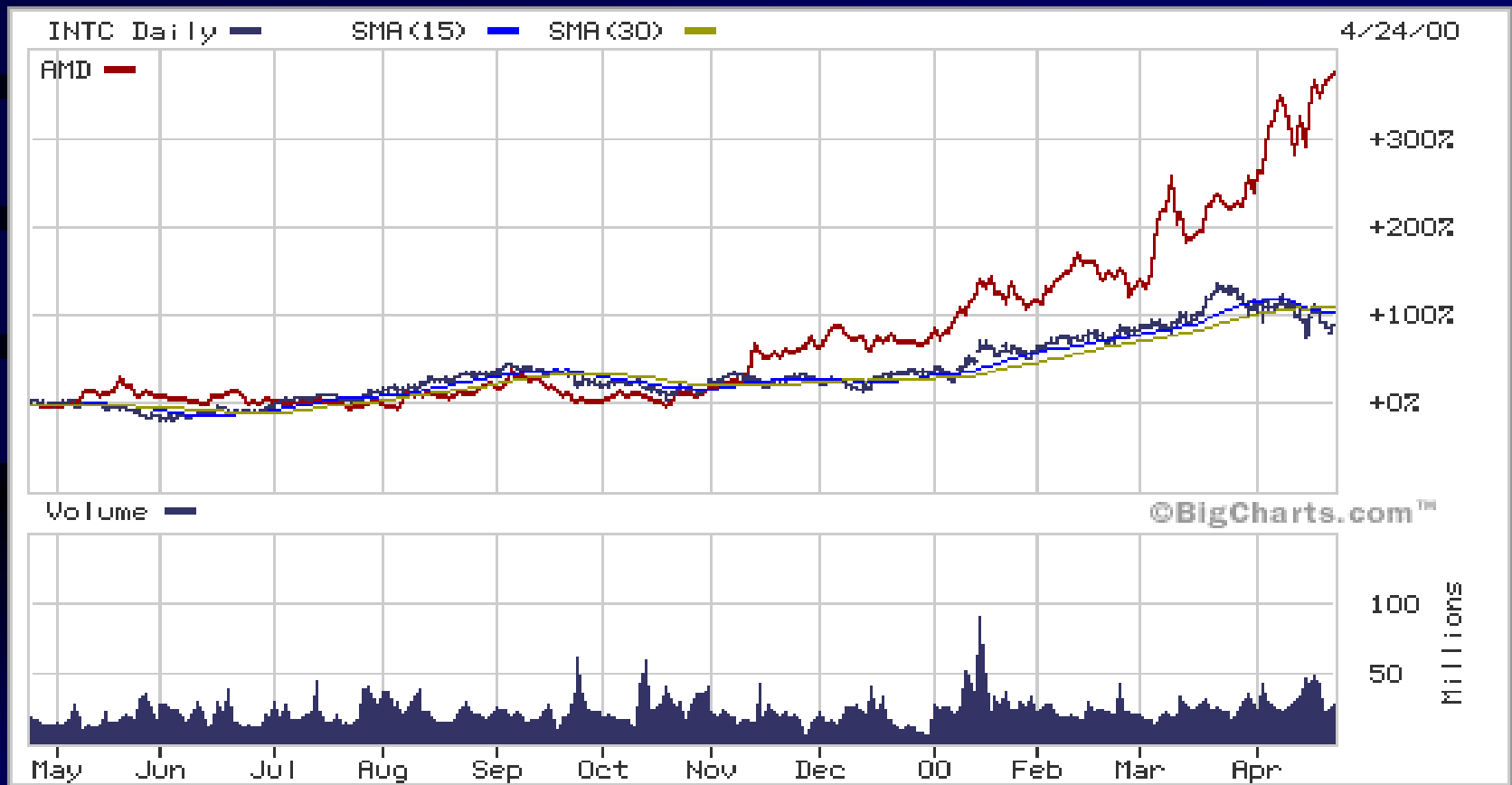


Application Notes

- Moving Average
 - Stock price
- Low-Pass Filter
 - SCADA
 - Trending



AMD Moves Above Intel!

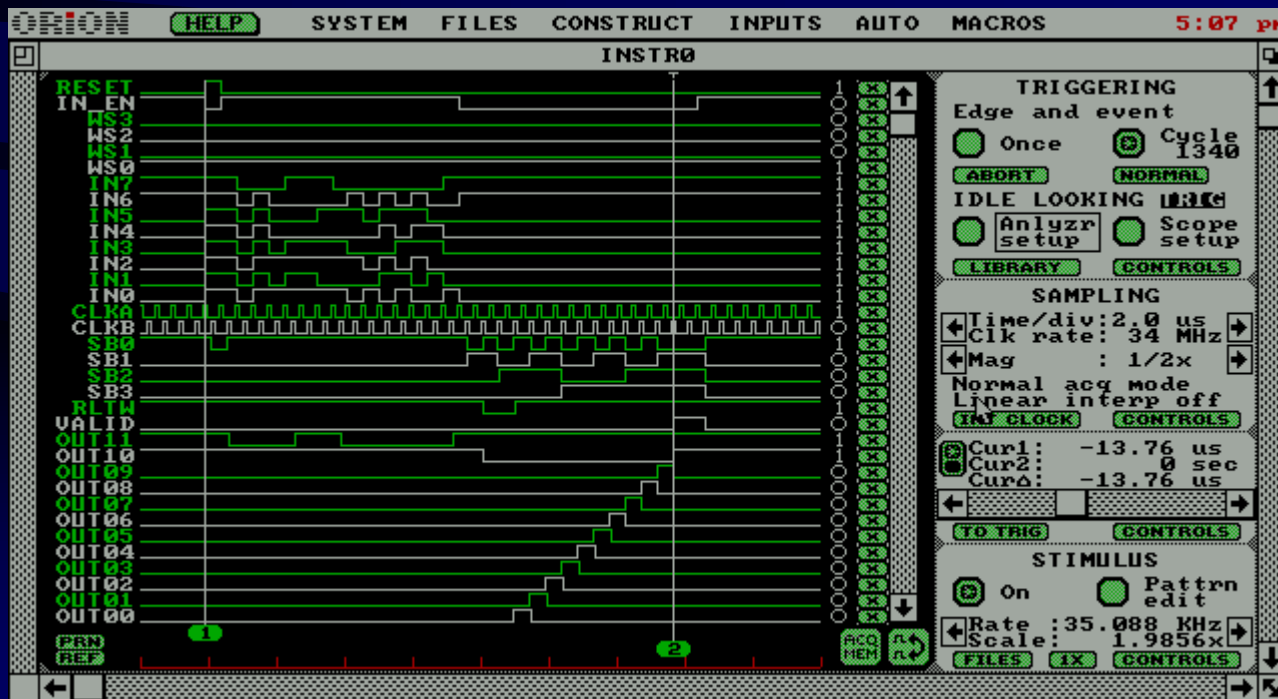


Testing Methodology

- Many short (4 – 5 input, 2 – 3 window size) pre-test vectors were used to ascertain ASIC functionality.
- Fifteen extensive test vectors, each for one of the fifteen window sizes, that inputted numbers outside of the window size – tests proper addition of current inputs and subtraction of old inputs and division.

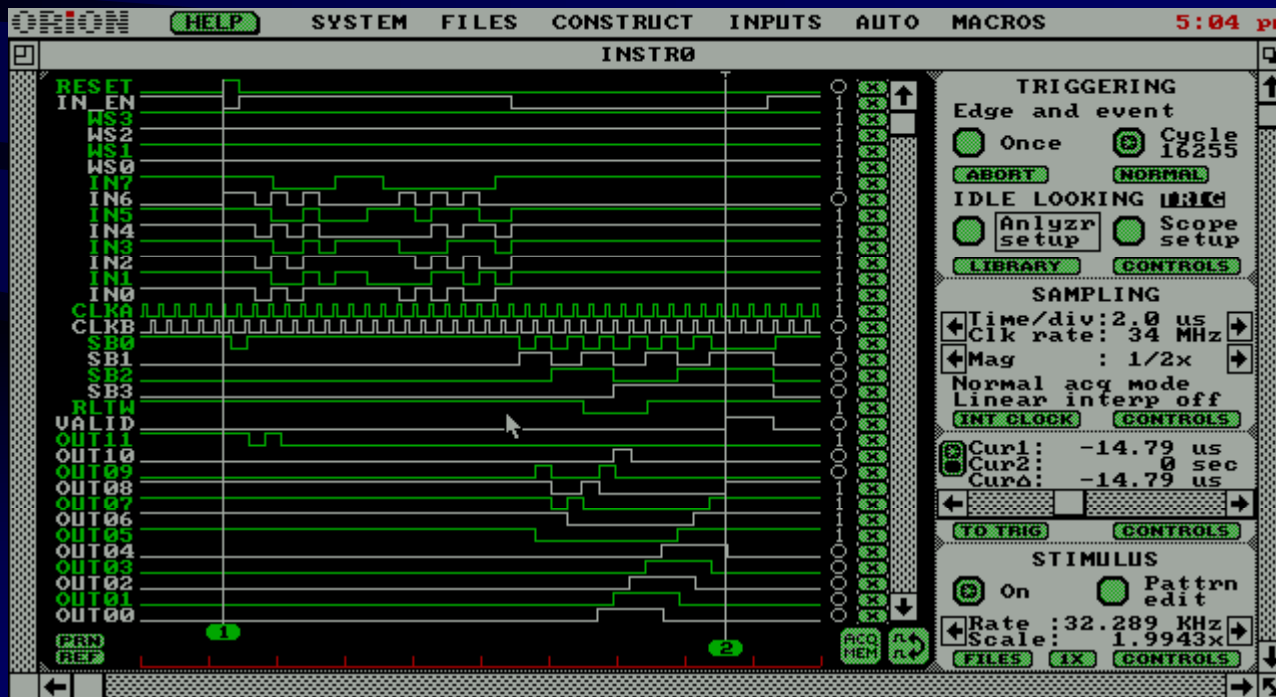
Sample Waveforms

Window Size = 1



Sample Waveforms (cont.)

Window Size = 15



ASIC Testing Results

- Chip 1
 - Works!
- Chip 2
 - Destroyed...
 - Inserted chip backwards (doh!)
 - 1 Vdd and 3 GND bonding wires burnt
- Chips 3, 4 and 5
 - All Work!

Maximum Speed

- Estimated clock speed: 13ns -> 76 MHz
- Actual clock speed: 2.16 MHz
- Division rate: 14.79 μ s for 15 inputs 67 KHz

MOSIS Fabrication Yield

- Four out of five of our chips tested successfully.
- The yield is either 80% or 100% -- we will never really know since we accidentally burned chip 2.
- If we had to put our money on it, we would say the yield is more likely 100%.