DETOL Verification

Multiprocessing Pipelined Matched Filter Architecture Using Online Arithmetic.

ELEC 423
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Outline

- Review of Functional Description
- Functional Test Results
- Speed Test Results
- Yield
Chip
### Functional Description: Pin Map

|   | SI@k0 | SI@k1 | SI@k2 | SI@k3 | Vdd | SI@k4 | Restart | Precision | Clock A | Clock B | GND | Out3 | Out2 | Out1 | N/C | Ready | Accum | Mode | Vdd | N/C | N/C | N/C | N/C |
|---|-------|-------|-------|-------|-----|-------|---------|-----------|---------|---------|-----|------|-----|-----|-----|-------|-------|-----|-----|-----|-----|-----|
| Ln[1]y[1] |       |       |       |       |     |       |         |           |         |         |     |      |     |     |     |       |       |     |     |     |     |     |
| Ln[1]x[2] |       |       |       |       |     |       |         |           |         |         |     |      |     |     |     |       |       |     |     |     |     |     |
| Ln[1]x[1] |       |       |       |       |     |       |         |           |         |         |     |      |     |     |     |       |       |     |     |     |     |     |
| GND       |       |       |       |       |     |       |         |           |         |         |     |      |     |     |     |       |       |     |     |     |     |     |
| N/C       |       |       |       |       |     |       |         |           |         |         |     |      |     |     |     |       |       |     |     |     |     |     |

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Functional Description

- Multiprocessing
  Pipelined Matched Filter architecture using online arithmetic
Functional Tests Performed

- Tests performed using TLA & Omnilab:
  - Full-precision (4-digit online output, 12-bit)
  - Fast Precision-1 (1-digit online output)
  - Full-matched filter mode
  - Online addition only (mult. bypassed)

- Goals:
  - Verify online multiplier functionality
  - Verify online adder functionality
  - Verify overall matched filter functionality
Functional Test Results

- **Successes:**
  - Online multiplier works properly
    - Very complex \(\Rightarrow\) Very gratifying!
  - Online adder works as designed
  - Proper transitions of the PLA states
  - Final Output:
    - Correct for Fast Precision-1

- **Flaw:**
  - Final Output incorrect for Full Precision
  - Suspected error: final adder receiving out-of-sync control signals (PLA load/clear of pipeline/adder registers)
Speed Test Results

- Highest usable clock frequency:
  - \( \approx 45 \text{ MHz} \Leftrightarrow \approx 22 \text{ns} \) clock period.
  - Glitching becomes excessive at 50MHz.
  - Roughly same as Spice analysis suggested: 42.18MHz
Testing Portfolio
Testing Portfolio: Mode-1 Full-Precision
Testing Portfolio: Mode-0 Full-Precision
Testing Portfolio: Mode-1 Precision-1
Testing Portfolio: Mode-1 Full-Precision
Testing Portfolio: Speed Test (f=10MHz)
Testing Portfolio: Speed Test (f=20MHz)
Testing Portfolio: Speed Test (f=50MHz)
Conclusions

- Work-around: Matched-filtering *still* possible using two multipliers on chip (thanks to redundancy in design)
- Using multi-chip configuration, can still achieve higher data-rate/longer spreading codes
- Yield: all 5 chips are working identically
Conclusions

SPREADING CODE LENGTH 8

FULL OPERATION MODE

DETOL

By-Pass Mode
(ADDER ONLY)

DETOL

By-Pass Mode
(ADDER ONLY)

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FULL OPERATION MODE

SPREADING CODE LENGTH 32
(HARD DETECTION)

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