Application-Specific Integrated Circuits

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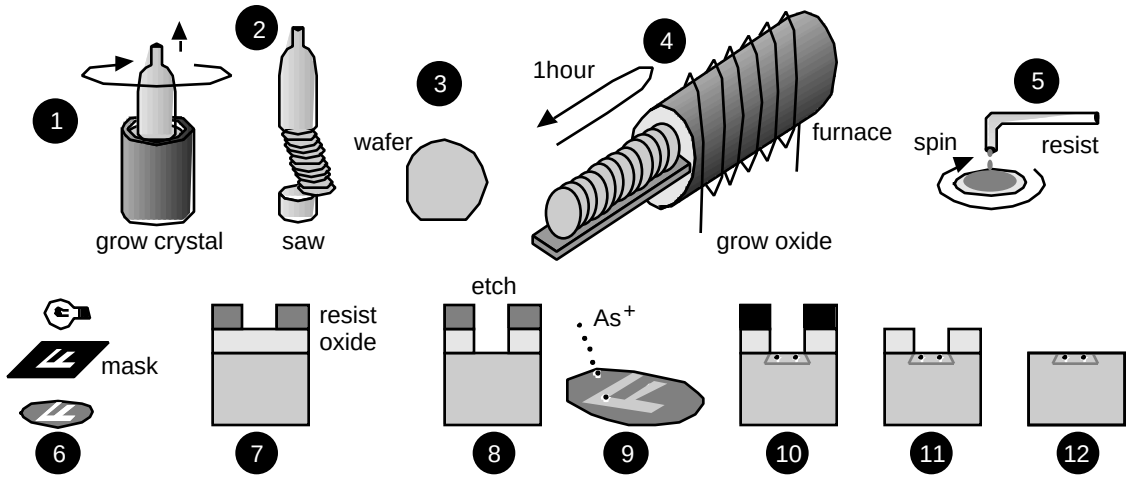
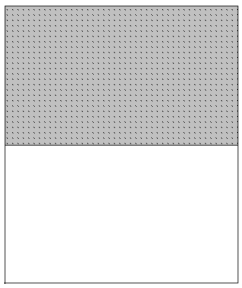
2.2 The CMOS Process



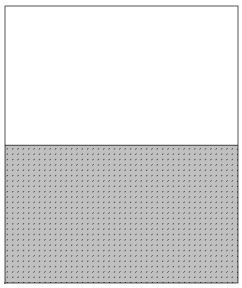
The CMOS manufacturing process

Key words: boule • wafer • boat • silicon dioxide • resist • mask • chemical etch • isotropic • plasma etch • anisotropic • ion implantation • implant energy and dose • **polysilicon** • chemical vapor deposition (CVD) • sputtering • photolithography • submicron and deep-submicron process • n-well process • p-well process • twin-tub (or twin-well) • triple-well • **substrate contacts** (well contacts or tub ties) • **active** (**CAA**) • **gate oxide** • **field** • field implant or channel-stop implant • **field oxide** (**FOX**) • bloat • dopant • **self-aligned process** • positive resist • negative resist • drain engineering • LDD process • lightly doped drain • LDD diffusion or LDD implant • stipple-pattern

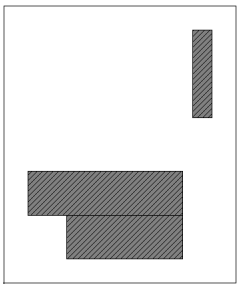
Mask/layer name	Derivation from drawn layers	Alternative names for mask/layer	Mask label
n-well	=nwell	bulk, substrate, tub, n-tub, moat	CWN
p-well	=pwell	bulk, substrate, tub, p-tub, moat	CWP
active	=pdiff+ndiff	thin oxide, thinox, island, gate oxide	CAA
polysilicon	=poly	poly, gate	CPG
n-diffusion implant	=grow(ndiff)	ndiff, n-select, nplus, n+	CSN
p-diffusion implant	=grow(pdiff)	pdiff, p-select, pplus, p+	CSP
contact	=contact	contact cut, poly contact, diffusion contact	CCP and CCA
metal1	=m1	first-level metal	CMF
metal2	=m2	second-level metal	CMS
via2	=via2	metal2/metal3 via, m2/m3 via	CVS
metal3	=m3	third-level metal	CMT
glass	=glass	passivation, overglass, pad	COG



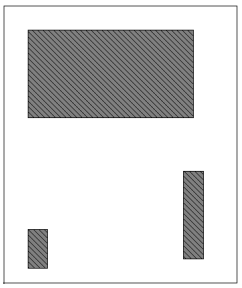
(a) nwell



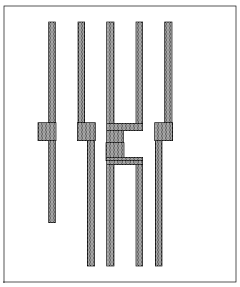
(b) pwell



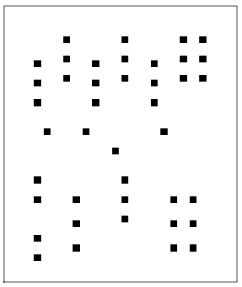
(c) ndiff



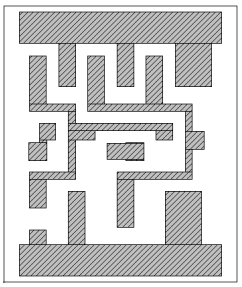
(d) pdiff



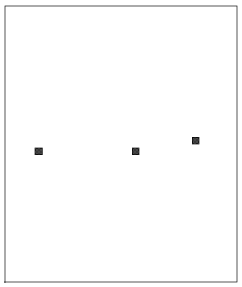
(e) poly



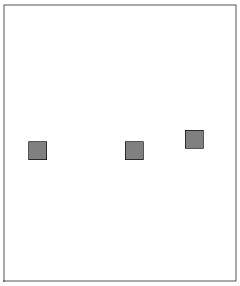
(f) contact



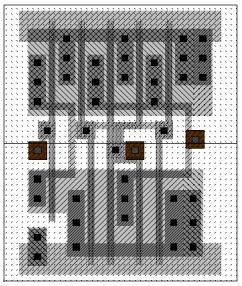
(g) m1



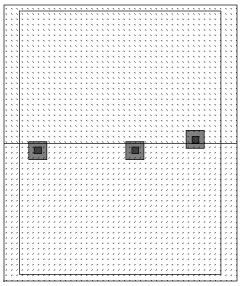
(h) via



(i) m2



(j) cell



(k) phantom

The mask layers of a standard cell

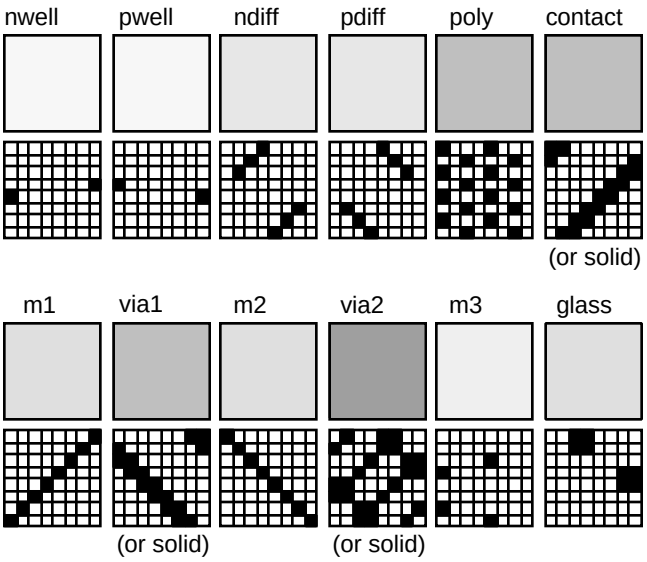
Active *mask*
CAA (mask) = ndiff (drawn) pdiff (drawn)

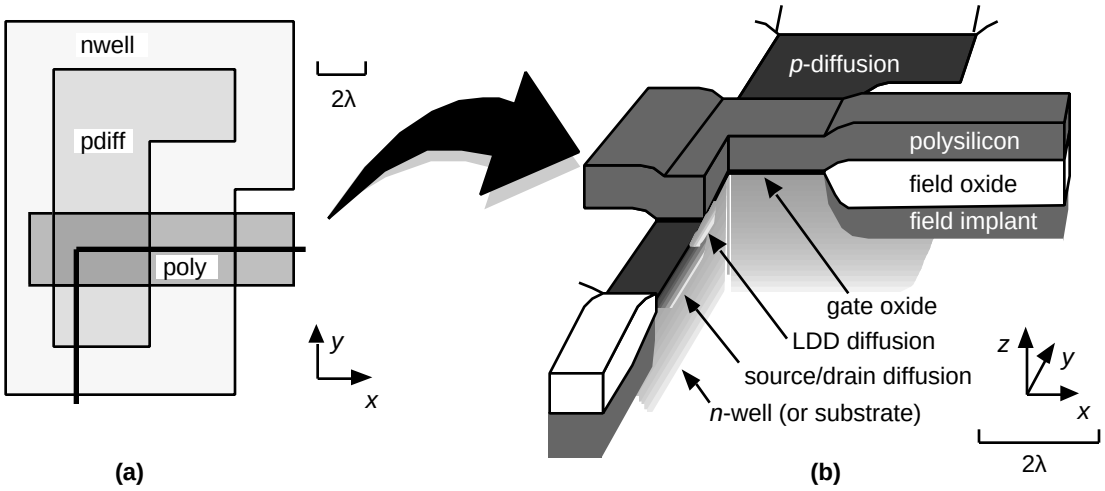
Implant select *masks*
CSN (mask) = grow (ndiff (drawn)) and
CSP (mask) = grow (pdiff (drawn))

Source and drain diffusion (on the *silicon*)
n-diffusion (silicon) = (CAA (mask) CSN (mask)) (¬ CPG (mask)) and
p-diffusion(silicon)=(CAA(mask) CSP(mask)) (¬ CPG(mask))

Source and drain diffusion (on the *silicon*) in terms of *drawn* layers
n-diffusion (silicon) = (ndiff (drawn)) (¬ poly (drawn)) and
p-diffusion (silicon) = (pdiff (drawn)) (¬ poly (drawn))

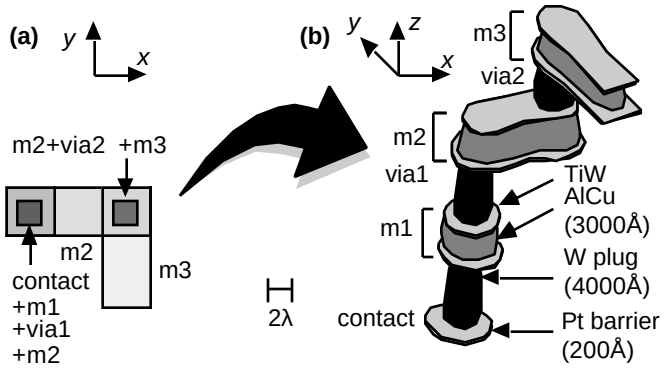
Drawn layers and stipple patterns





The transistor layers

The interconnect layers



2.2.1 Sheet Resistance

Sheet resistance (1μm)			**Sheet resistance (0.35μm)**		
Layer	**Sheet resistance**	**Units**	**Layer**	**Sheet resistance**	**Units**
n-well	1.15± 0.25	kΩ/square	n-well	1± 0.4	kΩ/square
poly	3.5± 2.0	Ω/square	poly	10± 4.0	Ω/square
n-diffusion	75± 20	Ω/square	n-diffusion	3.5± 2.0	Ω/square
p-diffusion	140± 40	Ω/square	p-diffusion	2.5± 1.5	Ω/square
m1/2	70± 6	mΩ/square	m1/2/3	60± 6	mΩ/square
m3	30± 3	mΩ/square	metal4	30± 3	mΩ/square

Key words: **diffusion** • **Ω/square** (ohms per square) • **sheet resistance** • **silicide** • self-aligned silicide (**salicide**) • **LI**, white metal, local interconnect, metal0, or m0 • **m1** or metal1 • **diffusion contacts** • **polysilicon contacts** • **barrier metal** • **contact plugs** (**via plugs**) • **chemical–mechanical polishing** (**CMP**) • **intermetal oxide** (**IMO**) • **interlevel dielectric** (**ILD**) • **metal vias**, **cuts**, or **vias** • **stacked vias** and **stacked contacts** • **two-level metal** (**2LM**) • **3LM** (**m3** or metal3) • **via1** • **via2** • **metal pitch** • **electromigration** • **contact resistance** and **via resistance**