4

Verifying the Multiplexer Layout

This chapter introduces you to interactive verification. You will perform two different tests in the Virtuoso® layout editor while using Assura™ interactive verification products. One test uses the Design Rule Checker (DRC) to compare your design against the design rule, and the other test uses Layout Versus Schematic (LVS) software to check your design's connectivity. You will be

When you finish this chapter, you will be able to

- Run a design rule check and view errors
- View and correct DRC errors
- Run extraction on a layout

- View a schematic
- Cross-probe between a layout and a schematic
- Rerun verification after correcting an error

Finding Out if You Can Run Interactive Verification

You might not have a license to run the interactive verification products.

➤ Click the *Verify* menu to find out whether you can use interactive verification.

If the commands under *Verify* appear shaded, you do not have a license to run interactive verification. You can either read this chapter to get an idea about how interactive verification works, or you can go on to the next chapter.

If You Have Not Completed the Previous Chapters

This chapter assumes you have followed the steps in the previous chapters. If you have, you can skip this section and go to the "Creating a Test Case for Checking Errors" on page 4-5. If you did not follow the steps in the previous chapters, you must copy a completed design from the `master` library so you can go through this chapter. The following steps show you how to copy the completed design from the `master` library.

It is possible to run out of resources, such as memory, if you run multiple layout editors. Before you start the software, you need to check whether the software is already running.

1. Type the following in an xterm window to check whether the layout editor is already running:

   ```
   ps auxw | grep layout
   ```

2. If the layout editor is running, choose *File – Exit* in the Command Interpreter Window (CIW) to exit the software.

3. Type the following in an xterm window to start the layout editor:

   ```
   cd ~/cell_design
   layoutPlus &
   ```

4. Choose *File – Open.*

5. Type the library, cell, and view names as follows:

Library Name	`master`
Cell Name	`mux2`
View Name	`layout`

6. Click *OK*.

   The *mux2* cell from the `master` library opens.

7. In the cellview window, choose *Design – Save As.*

   The Save As form appears.

8. In the Save As form, type the library and cell names as follows:

Library Name	`tutorial`
Cell Name	`mux2`

9. Click *OK*.

The *mux2* cell is copied to the `tutorial` library.

10. In the *mux2* cellview, choose *Window – Close* to close the cellview.

11. In the CIW, choose *Open – File* to open the *mux2* layout you just saved.

12. Type the library, cell, and view names as follows:

Library Name	`tutorial`
Cell Name	`mux2`
View Name	`layout`

13. Click *OK*.

The *mux2* cell from the `tutorial` library opens.

Note: Another way to open a cellview is with the *Open* command. Using *Open* replaces the current window with the new window. To use the *Open* command, choose *Design – Open.* The Open File form appears. Set the library, cell, and view names to the cellview you want to open, and click *OK.* The current cellview is replaced with the new cellview.

Creating a Test Case for Checking Errors

If you followed the instructions in the last chapter exactly or copied the *mux2 layout* from the `master` library, the multiplexer design does not generate any verification errors. In this section, you will make a small, deliberate error on the *metal1* layer so you can learn how to display and correct errors.

In this section, you learn to

- Turn off visibility of all layers except *metal1* so it is easier to see the path you edit
- Make an error by stretching the end of a path
- Turn visibility of all layers back on

Displaying Only the metal1 Layer

Open your *mux2* layout if you closed it after the last chapter. To make it easier to see the path you want to edit, you turn off visibility of all layers except *metal1.*

1. In the Layer Selection Window (LSW), press `Shift` and click middle on the *metal1 dg* layer.

   The *metal1* entry layer is now the current entry layer. The layer names in the LSW are all shaded gray to show they are invisible, with the exception of *metal1*.

   The *mux2* layout window does not change. You must redraw the window to see any changes you make in the LSW.

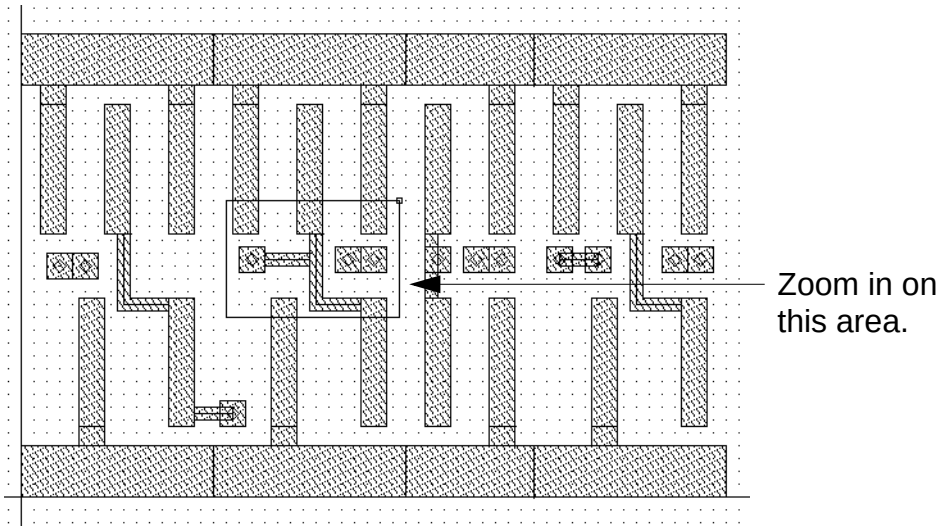
2. Move the cursor to the layout window and press `Control-r`.

Now you see only *metal1* objects in the layout window.

Stretching a Path

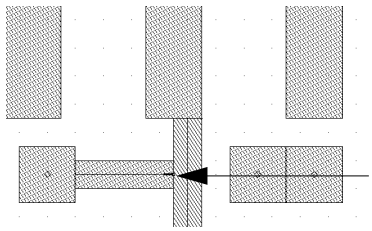
In this section, you learn how to stretch a path.

1. Zoom in on the area shown below.



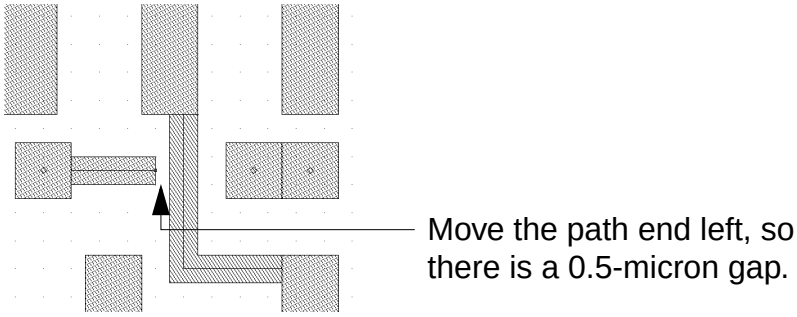
2. Press the s key to open the Stretch form.
3. Click the right end of the *metal1* path.

The entire path is highlighted. Bolder highlighting appears at the endpoint. The bold mark shows you selected the end of the path.



4. Stretch the path so there is a 0.5-micron gap by clicking X = 33, Y = 28.

The display grid points are each 1 micron apart. The cursor snaps to the grid every 0.5 microns. The gap you create is one-half of one visible grid space.



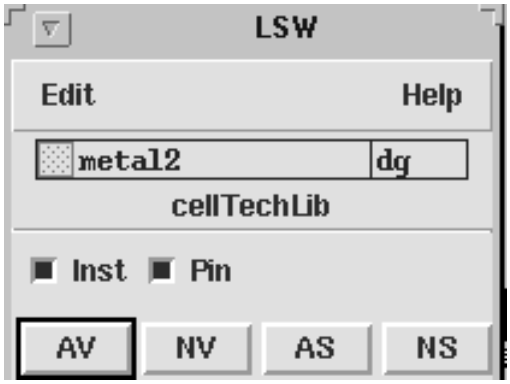
5. Press the Escape key to stop the *Stretch* command.

You just created an error by stretching the path. Later you use DRC to find this error.

Redisplaying All Layers

It is not necessary to view all the layers when you run DRC. However, errors are easier to see with all layers visible.

1. In the LSW, click *AV* (All Visible).



2. Move the cursor into the layout window and press `Control-r` to see all layers.

Performing a Design Rule Check

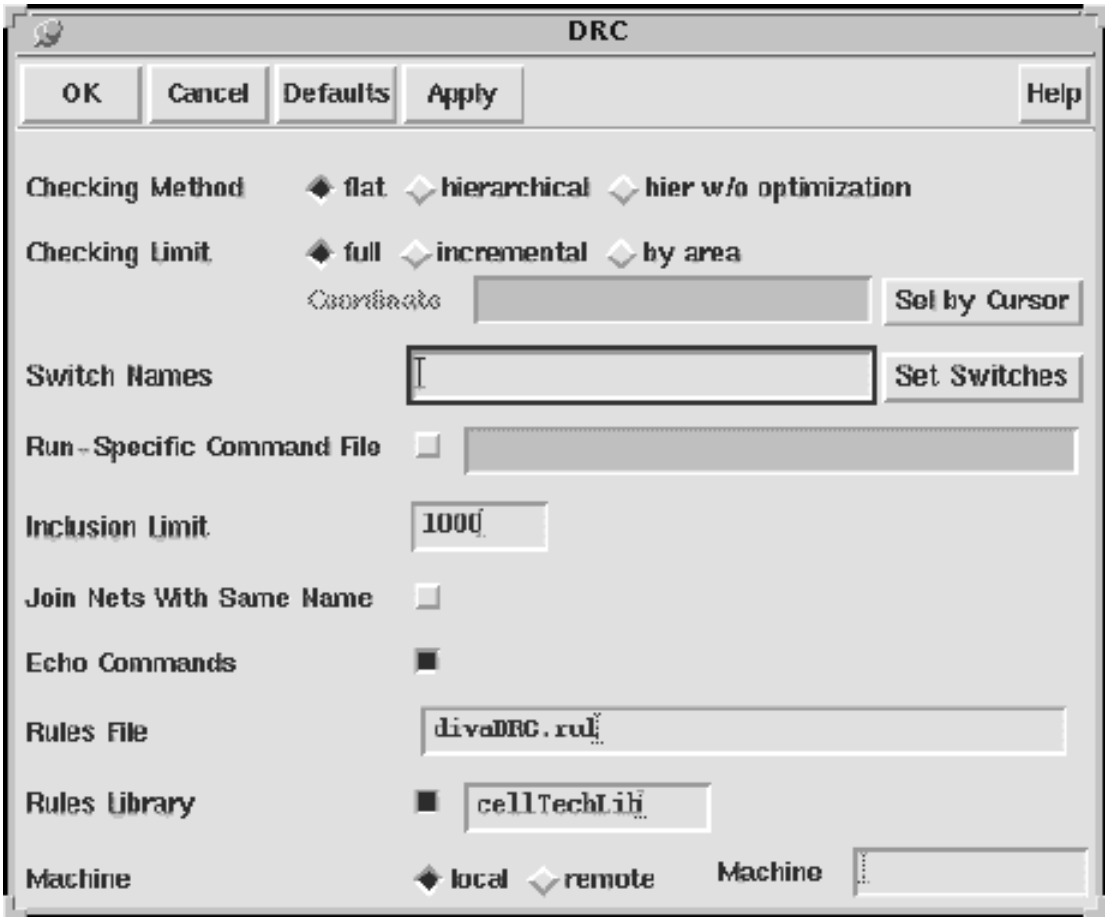
DRC checks your layout against physical design rules defined in the `divaDRC.rul` file located in the `cellTechLib` directory. This section shows you how to

- Run DRC to search for errors
- Display information about any errors

Running DRC

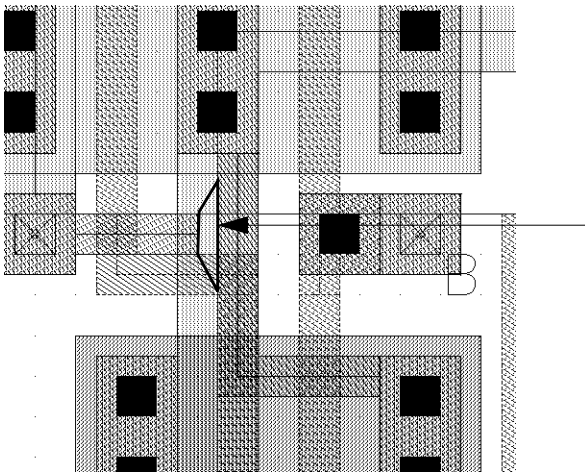
1. Choose *Verify – DRC*.

   The DRC form appears.



2. Click *OK* to run DRC.

The CIW reports one error. A blinking polygon, called an error flag, appears at the location of the error.



Important

Do not correct this error yet. You will run LVS later in this chapter to see how LVS reports this same error.

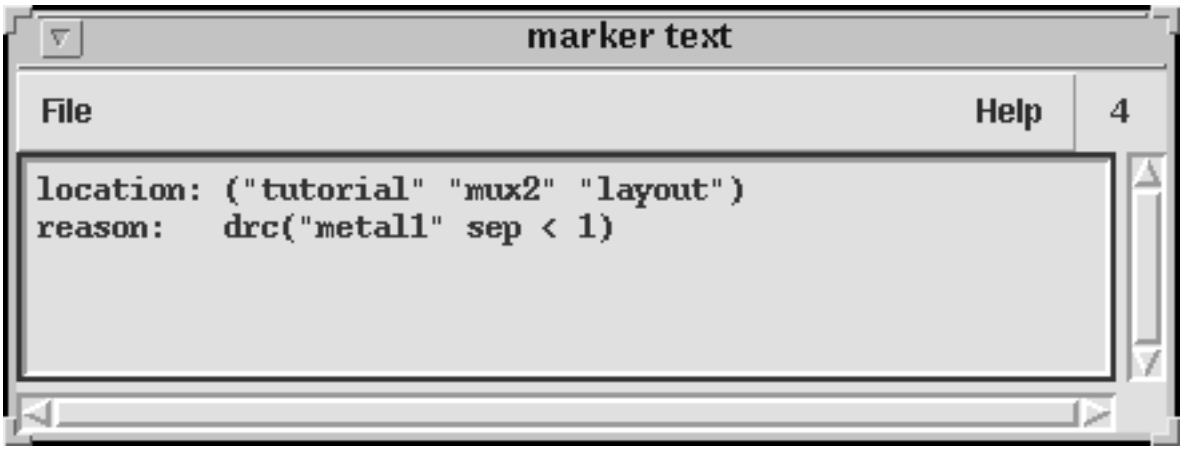
3. Press the f key to fit the entire design in your window, and look for any other errors you might have made.
4. If you have any other errors, correct them by redrawing the flagged objects using instructions in the previous chapters. Run DRC again before proceeding.

Viewing Errors

Use the *Markers – Explain* command to display more information about the error flagged by DRC.

1. In the *mux2* cellview window, choose *Verify – Markers – Explain*.
2. Click the error flag.

   The error flag is highlighted in yellow to show that you selected it. A window appears at the top left of the screen. It lists the cellview containing the error and the rule that was violated.



   In the CIW, DRC reports a spacing violation:

```
"metal1" sep < 1 (metal1 separation is less than 1 micron).
```

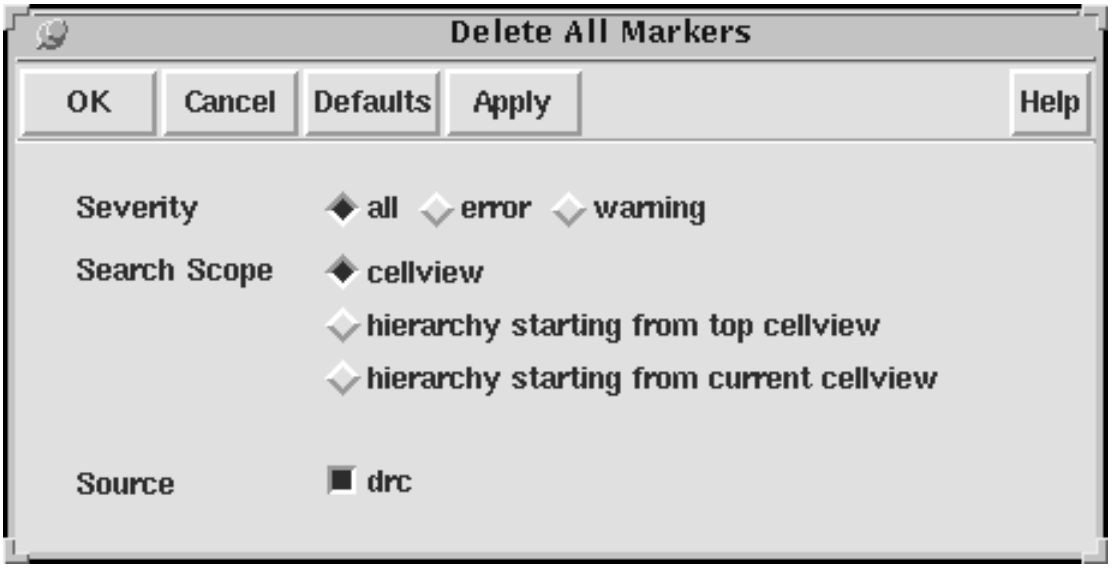
   Even though the two paths should be connected, DRC reports a spacing violation because the spacing between objects on the *metal1* layer should be 1.0 microns and the space between the two paths on *metal1* is 0.5 microns.

3. Press the Escape key to cancel the *Explain* command.

   If there were more error flags, you could continue to use *Explain* to explain the other errors.

4. Choose *Verify – Markers – Delete All* to remove the error marker.

   The Delete All Markers form appears.



5. Click *OK*.

   The error marker is removed.

Extracting Connectivity from the Layout

You must extract the connectivity from the layout cellview to compare the layout and schematic cellviews. To extract connectivity, you run the Extract program.

The Extract program uses rules defined in the technology file to recognize devices and establish electrical connections (nets).

The Extract program creates a temporary cellview, called the extracted view, that shows the nets. You will use both the extracted cellview and the layout cellview in this section.

Important

As you follow the steps in the rest of this chapter, be careful to use the correct cellview. Check the title banner for the view name *layout* or *extracted*.

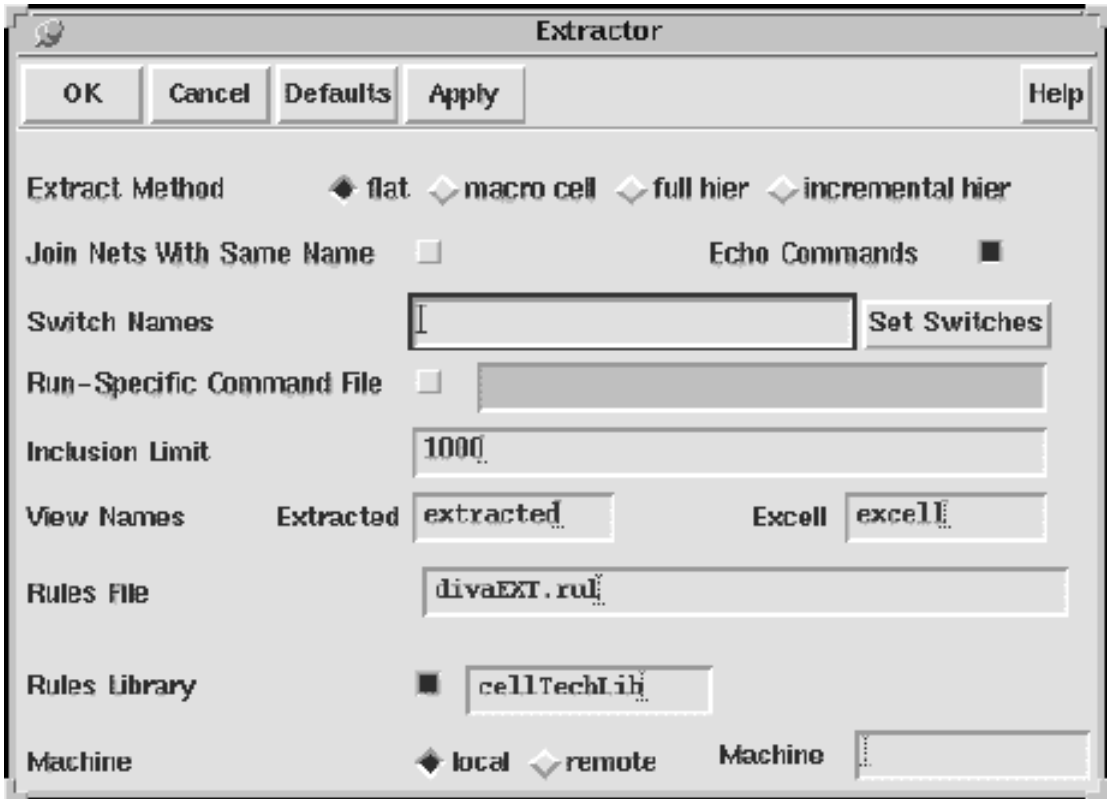
In this section, you learn to

- Use the *Extract* command to create an extracted view of *mux2*
- View the extracted data

Extracting the Layout

1. Choose *Verify – Extract*.

The Extractor form appears.



Note: If you are running the Analog Artist® design system, the Extractor form is different than the form that appears here. You can continue this tutorial despite the different form. If you want detailed descriptions of options that appear in Analog Artist forms, refer to the *Assura® Diva Verification Reference* manual.

2. Turn on *Join Nets With Same Name*. This will merge nets with the same names while suppressing warning messages about different nets that have the same name.

3. Click *OK* to run the Extract program.

   The extraction rules appear in the CIW as the extract program runs. When extraction is complete, you see

   ```
   saving rep tutorial/mux2/extracted
   ```

   This means the extracted cellview was created.

Viewing Extracted Data

The extracted view of *mux2* is similar to but not identical to the layout cellview. In this section, you look at the extracted cellview so you understand the differences between the extracted and the layout cellviews.

1. In the CIW, choose *File – Open* to view the extracted *mux2* view.

   The Open File form appears.

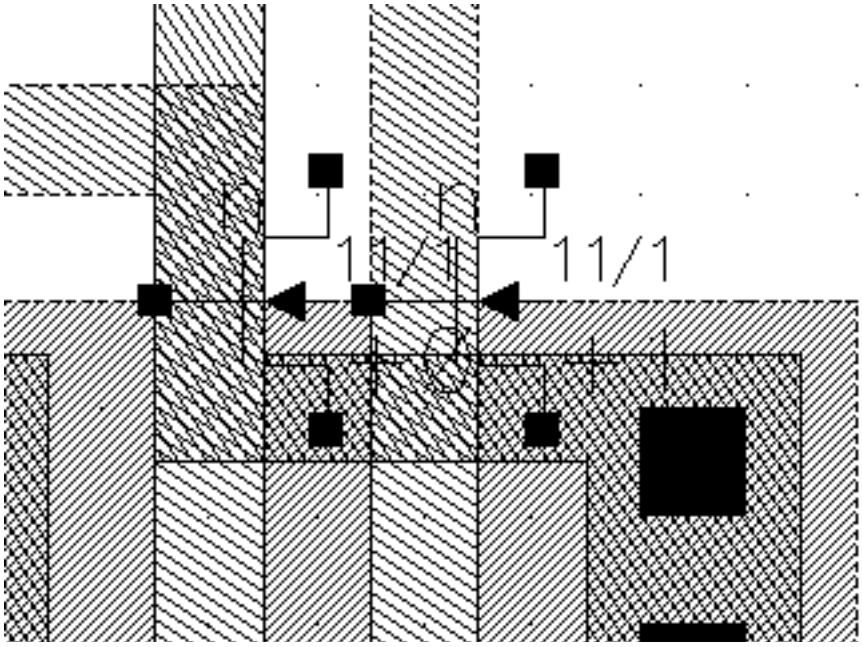
2. Type the library, cell, and view names as follows:

Library Name	`tutorial`
Cell Name	`mux2`
View Name	`extracted`

3. Click *OK*.

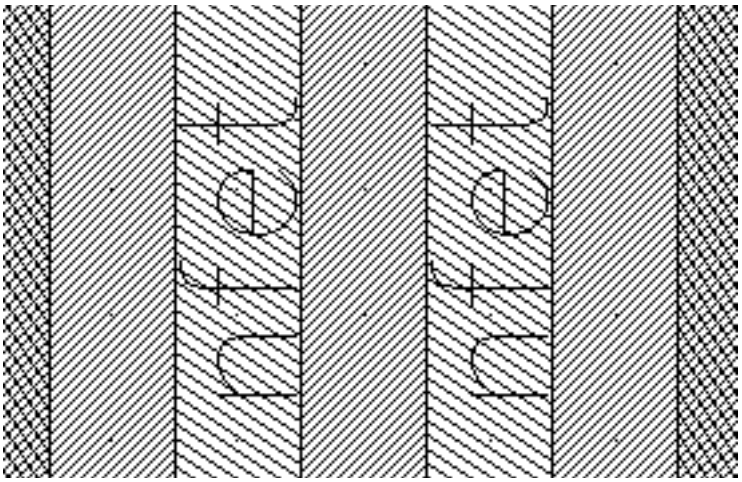
   The extracted cellview appears on top of the layout cellview. The banner contains the following:

The extracted cellview is similar to the layout, but the gates now have symbols at one end.



4. Press `Control-f` to display only level 0 data.

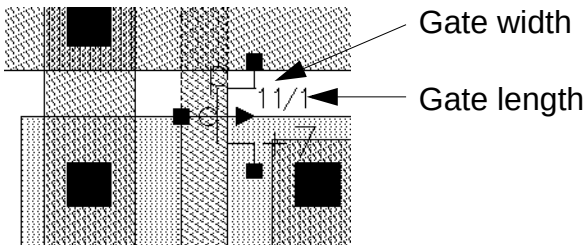
The gate symbols disappear, and you see a name inside each gate region. Each gate has been mapped to either an *nfet* or *pfet* device, identified by an instance of an *ivpcell*.



An *ivpcell* is a special parameterized cell used by the verification program to display devices.

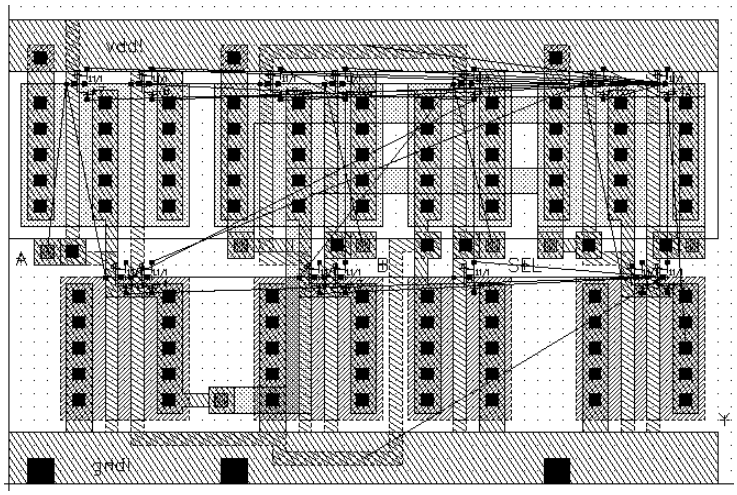
5. Press `Shift-f` to display all levels again.
6. Zoom in on one of the symbols.

   You see the gate width and length displayed next to the symbol.



7. Display the electrical connections by setting *Nets* on in the Display Options form. Press the e key to open the Display Options form.
8. Select *Nets*.
9. Click *Apply*.
10. Move the cursor into the extracted view and press the f key to fit the design in the window again.

    You see the electrical connections in the extracted cellview.



11. In the Display Options form, turn *Nets* off.
12. Click *OK* to close the Display Options form.

Comparing the Layout to the Schematic

The LVS program lets you compare the schematic to the physical layout so you can check for connectivity errors. LVS uses both the extracted cellview you created in the previous section and the schematic view of the multiplexer. This tutorial provides a schematic cellview for you.

In this section, you learn to

- Display the schematic cellview
- Run LVS

Displaying the Schematic View

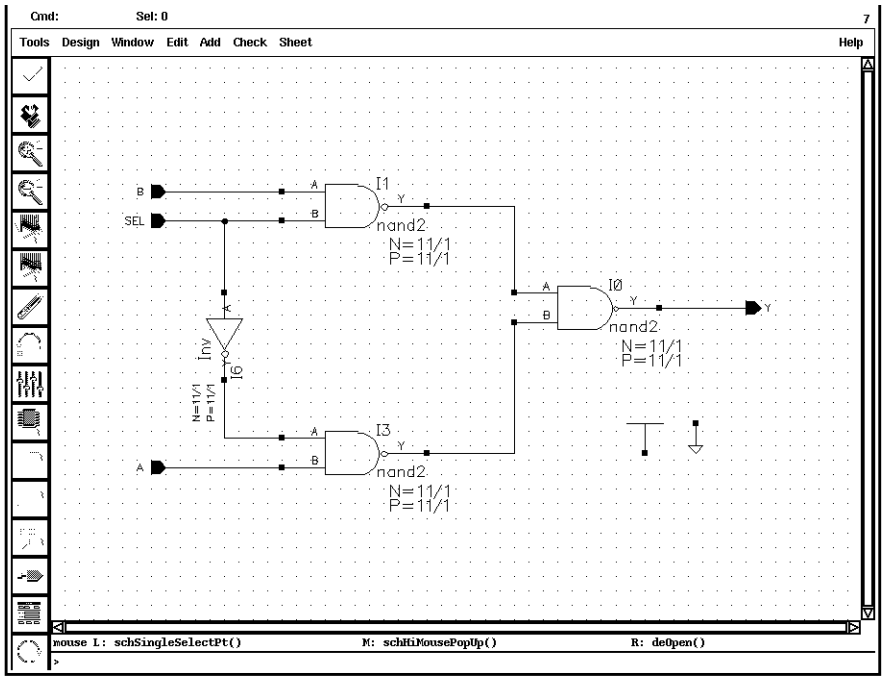
You will use the schematic for checking details between the schematic and layout after you run LVS. For now, you just need to be sure the schematic exists. You display the schematic to remind you of what LVS is using to check the design.

1. Choose *File – Open* to view the *mux2* schematic.
2. Type the library, cell, and view names as follows:

Library Name	`master`
Cell Name	`mux2`
View Name	`schematic`

3. Click *OK*.

The schematic cellview appears.

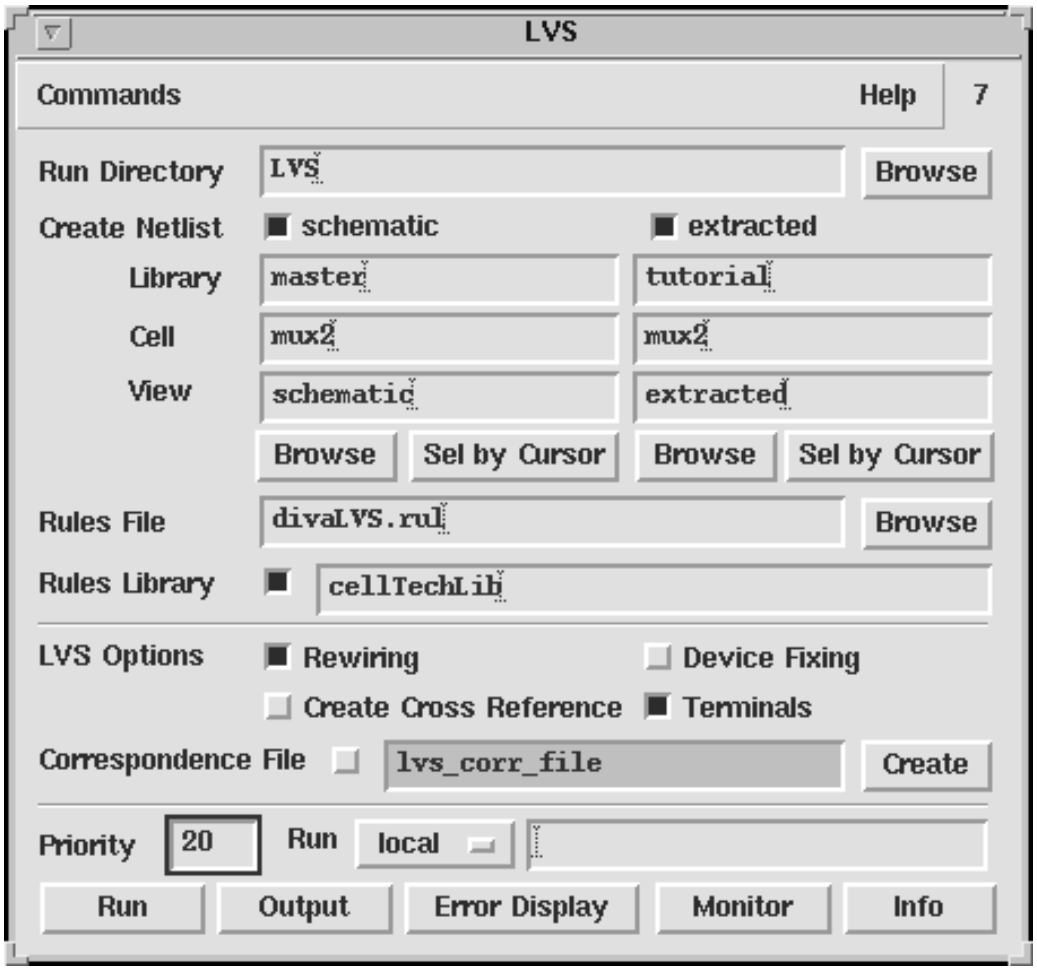


Note: To fit your windows on your screen, click and hold on any corner of the schematic window and drag the mouse until the window is a smaller size. Then press the f key in the schematic window to fit the schematic drawing within the resized window.

Running LVS

1. In the *mux2* extracted cellview, choose *Verify – LVS*.

The LVS form appears.



Note: If you are running the Analog Artist design system, the LVS form is slightly different than the form that appears here. You can continue this

tutorial despite the different form. If you want detailed descriptions of options that appear in Analog Artist forms, refer to the *Assura® Diva Verification Reference* manual.

2. Fill in the schematic fields in the LVS form by clicking the *Sel by Cursor* button under the schematic fields, then click left in any area of the schematic cellview window.

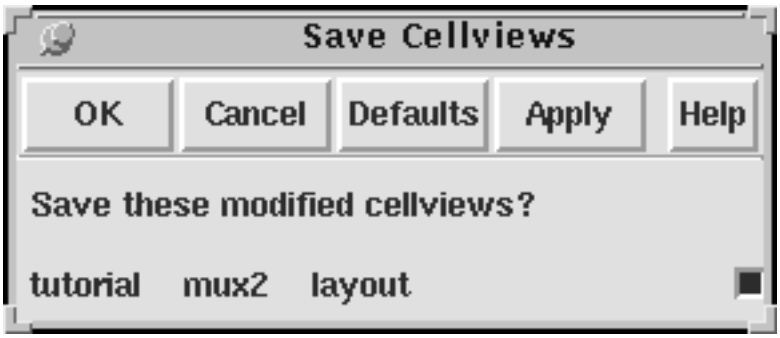
   The schematic fields are filled in with `master`, `mux2`, and `schematic`.

3. Set the *Priority* field to `20`.

   The Priority default is 0. Priority 0 slows down other actions on the system.

4. Click *Run* to start the LVS job.

   The Save Cellviews form appears, asking if you want to save the *mux2* layout cellview.



5. Click *OK* to save the *mux2* layout.

   The LVS job runs in the background and might take a couple of minutes to complete. When the job is finished, you see a dialog box, entitled Analysis Job Succeeded, telling you the job succeeded.

6. In the dialog box, click *OK*.

Note: If the dialog box says your job did not get completed, click *Info* in the LVS form and look at the log. The log tells you what caused the job to be terminated and when.

Analyzing LVS Errors

Now that you have run LVS, you can display information about the comparison between the schematic and the layout. Because you deliberately added a small error to the layout, LVS will report the discrepancy.

You can use the probe commands on the *Verify* menu to highlight any nets, including nets that LVS lists as having errors. You can perform either a single probe to highlight a net in the extracted cellview or a cross-probe to highlight a net in both the extracted and the schematic cellviews.

In this section, you learn to

- Display the LVS report
- Display the errors LVS found
- Probe and cross-probe between the schematic and extracted cellviews

Displaying an LVS Report

1. In the LVS form, click *Output*.

   A text window listing the output from the LVS run appears.

2. Scroll until you see the section that compares the layout and schematic.

LVS reports this information:

```
The net-lists failed to match.
```

You see LVS found 13 nets in the layout but only 12 in the schematic. It reports a net in the layout should be merged because the layout and schematic would match if two separate nets in the layout were connected (merged). Because the error you created was a disconnection within a net, this suggestion makes sense.

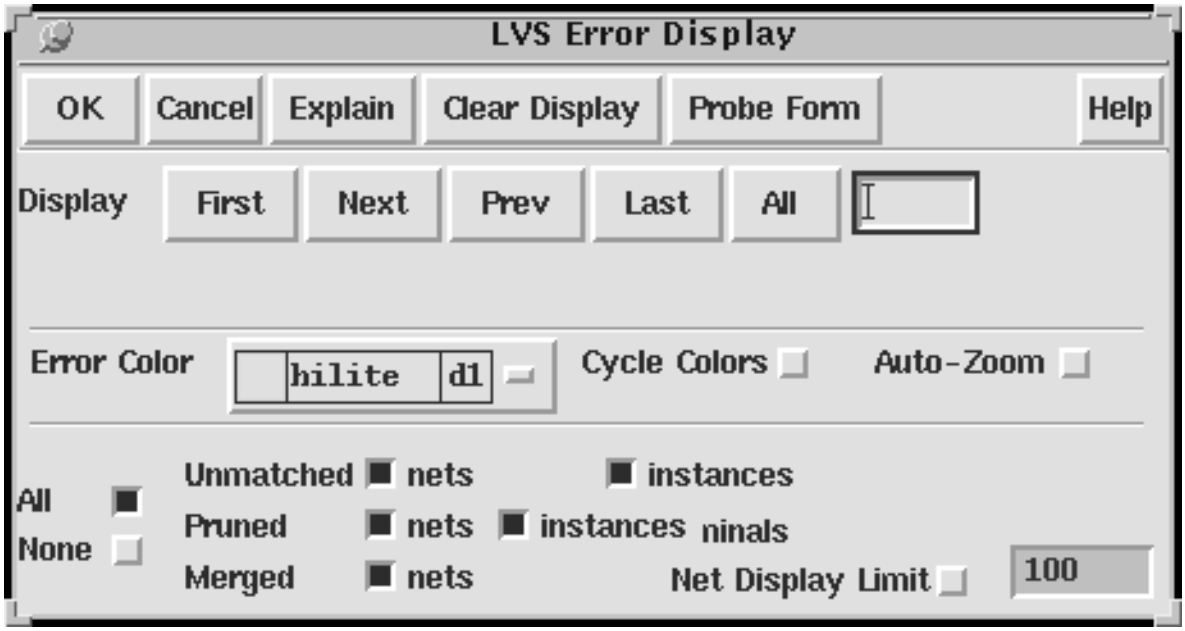
```
The net-lists failed to match.

                          layout  schematic
                             instances
        un-matched             0       0
        rewired                0       0
        size errors            0       0
        pruned                 0       0
        active                14      14
        total                 14      14

                               nets
        un-matched             0       0
        merged                 1       0
        pruned                 0       0
        active                13      12
        total                 13      12
```

3. In the report window, choose *File – Close Window*.

Displaying the Errors

1. At the bottom of the LVS form, click *Error Display*.

   The LVS Error Display form appears.

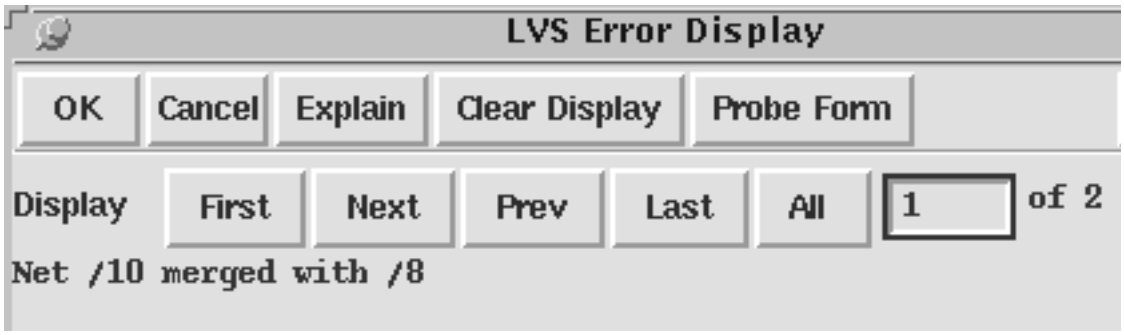


2. Move the cursor into the extracted window and press the `Escape` key.

   This makes the extracted window the current window. LVS displays the errors in the current window.

3. In the LVS Error Display form, click *First* in the *Display* field.

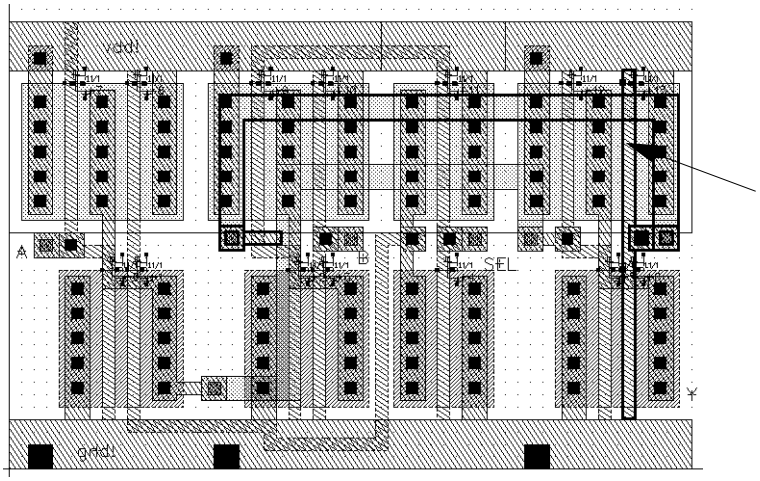
The LVS Error Display form displays a message indicating that two of the nets should be merged.



Note: LVS assigns numbers to the unlabeled nets. The numbers it assigns to your nets might not be identical to the net numbers shown above. Substitute the numbers on your LVS Error Display form in the following instructions.

In addition to the LVS Error Display form showing the nets to be merged, the geometries in the extracted layout that do not match anything in the

schematic are highlighted in yellow. In this case, LVS highlights the objects on the part of the net you disconnected.



4. In the LVS Error Display form, click *Clear Display*.

Probing the Schematic and Layout

To look at the nets LVS suggests you merge, you probe the schematic and extracted cellviews to highlight the nets. This section shows you how to

- Perform a single probe to highlight a net in the extracted cellview.

  You probe only the extracted view for net 10, which LVS found in the layout but not in the schematic.

- Perform a cross-probe to highlight a net in both the schematic and extracted cellviews.

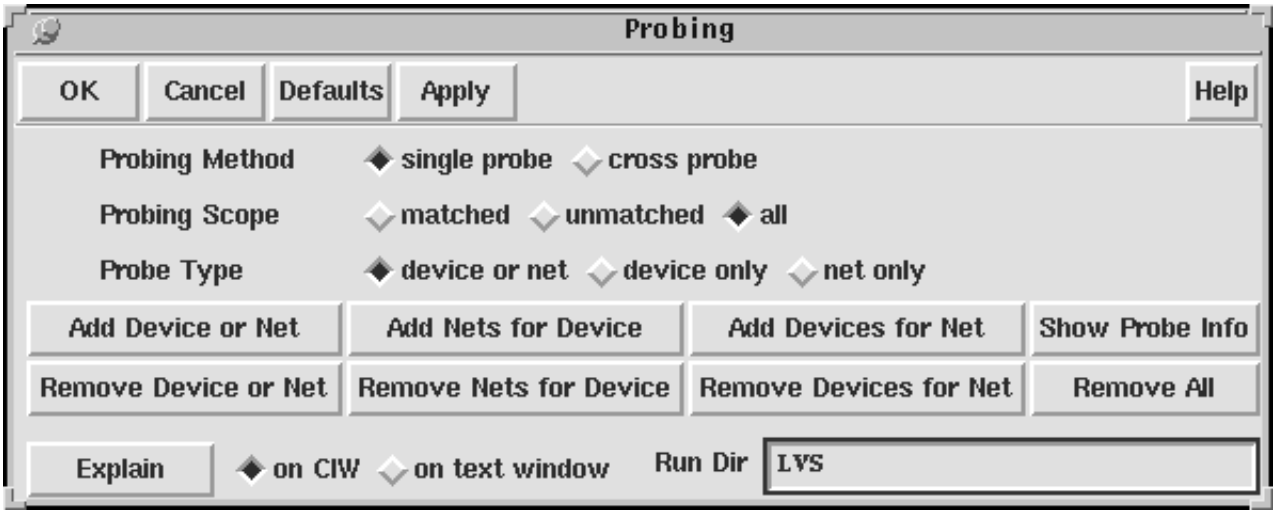
You probe both views for net 8, which LVS found in both the layout and the schematic.

1. In the LVS Error Display form, click *Probe Form*.

   The Probing form appears.

   Note: If you are running Analog Artist, the Probing form is different than the form that appears here. You can continue this tutorial despite the different form. If you want detailed descriptions of options that appear in Analog Artist forms, refer to the *Assura® Diva Verification Reference* manual.

2. Click *Add Device or Net*. If you are running Analog Artist, click *Add Net*.



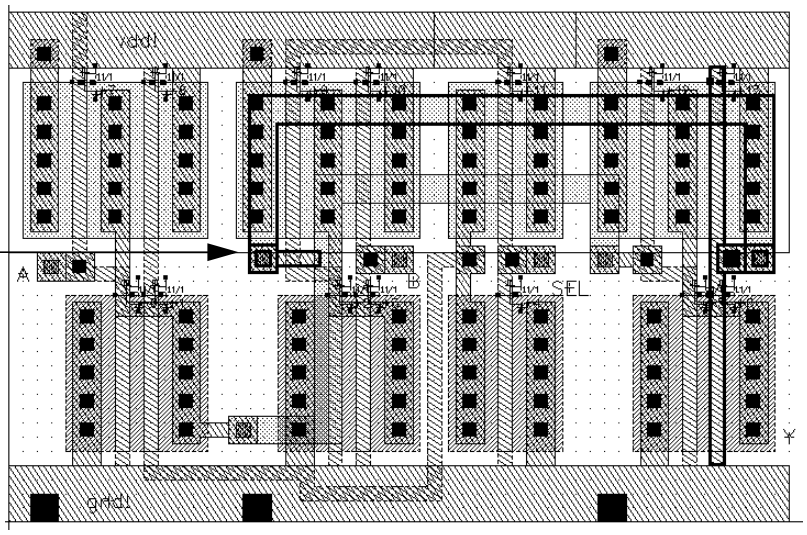
   By default, the form is set to perform a single probe. You first probe the extracted view for net 10.

3. In the CIW, type the net name, `"10"`, enclosed in quotation marks, and press `Return`.

Note: Several warning messages appear in the CIW, these do not have any effect on your probe.

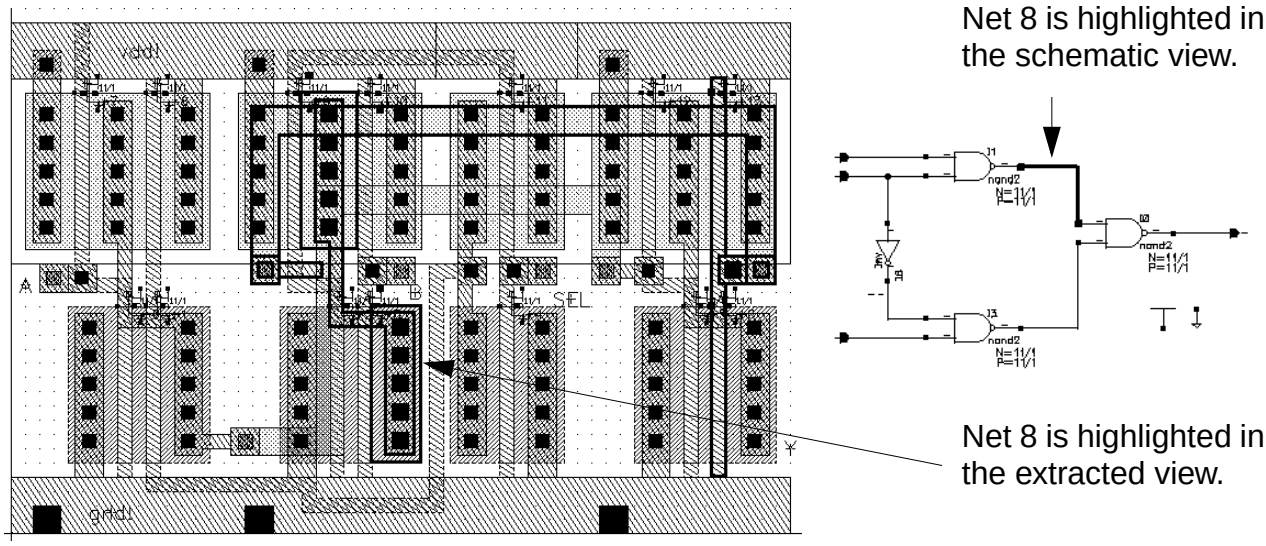
The shapes in net 10 are highlighted in yellow.

Net 10 is highlighted in the extracted view.



4. In the Probing form, change *Probing Method* to *cross probe*. If you are running Analog Artist, change the Probing Method to *cross probe matched*.
5. Click *Add Device or Net*.
6. Move the schematic cellview to the front of your screen so you can see its contents.
7. In the CIW, type the net name, `"8"`, enclosed in quotation marks, and press `Return`.

The shapes in net 8 are highlighted in yellow in both the extracted and schematic views.



8. To remove the probe highlights, in the Probing form, click *Remove All*.

   Note: You can also probe from the schematic to the layout. After you open the Probing form, click a net in the schematic.

9. In the Probing form, click *Cancel*.

10. In the LVS Error Display form, click *Cancel*.

11. In the LVS form, choose *Commands – Close Window*.

    Now that you have determined where the error is, you do not need to see the schematic view anymore.

12. In the schematic cellview, choose *Window – Close*.

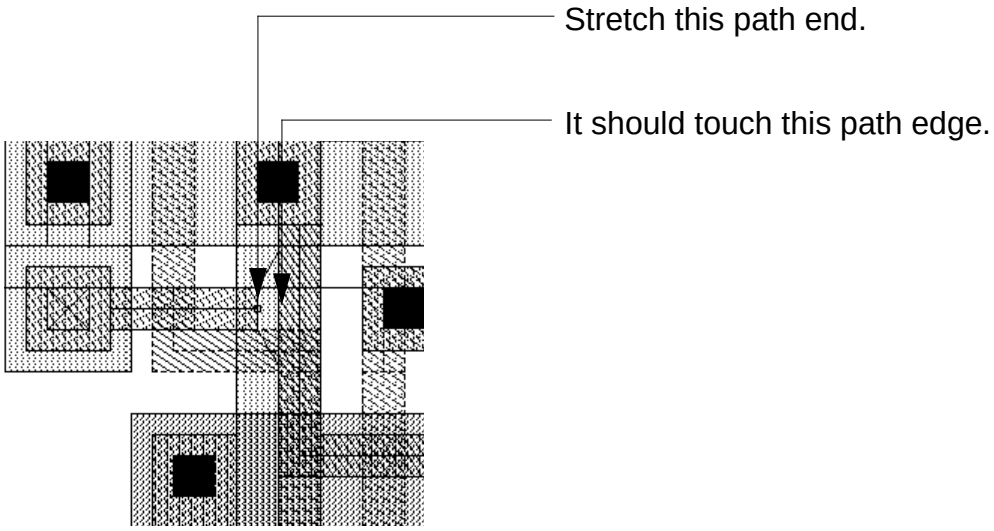
Correcting the Error

In the previous sections, you saw that the error both DRC and LVS discovered was caused by a break in one net in the layout. The break made it appear as if there were two nets. In this section, you correct the error and reconnect the net.

1. In the extracted cellview, choose *Window – Close*.

   The extracted cellview closes and you see the layout cellview. You always edit in the layout cellview and then reextract.

2. To correct the error in the layout cellview, press the s key and stretch the *metal1* path so it joins the two nets at point X = 33, Y = 28.



3. To stop the *Stretch* command, press the Escape key.

4. To save the layout cellview, in the icon menu, click the *Save* command icon.

The layout cellview is written to disk.

Rerunning Verification

After correcting the errors in the layout, you run verification again. The steps are nearly identical to those you followed earlier in this chapter, except this time you run an incremental DRC. This means you check only the changed portion of the design. The verification programs should not find any errors.

This section tells you how to

- Run an incremental DRC
- Run an extraction on a layout
- Run LVS from the extracted cellview

The instructions in this section are brief because you have already done the steps before. If you want more details, you can go back through the previous sections.

Running an Incremental DRC

The system keeps track of any changes you made since the last DRC. You can run an incremental DRC to check only your changes to the design. This makes the DRC go faster.

1. In the *mux2* layout window, choose *Verify – DRC* to display the DRC form.
2. Set *Checking Limit* to *incremental*.
3. Click *OK* to run DRC.

   When DRC has been completed, you see output in the CIW that there are 0 errors.

Reextracting the Layout

You must extract the layout again so the extracted view includes your correction.

1. In the *mux2* layout window, choose *Verify – Extract* to display the Extractor form.
2. In the Extractor form, click *OK*.

   Extraction is complete when you see this message in the CIW:

```
saving rep tutorial/mux2/extracted
******  Summary of rule violation for cell "mux2 layout" *******
    Total errors found: 0
```

3. In the CIW, choose *File – Open.*

   The Open File form appears.

4. Type the library, cell, and view names as follows:

Library Name	`tutorial`
Cell Name	`mux2`
View Name	`extracted`

5. Click *OK*.

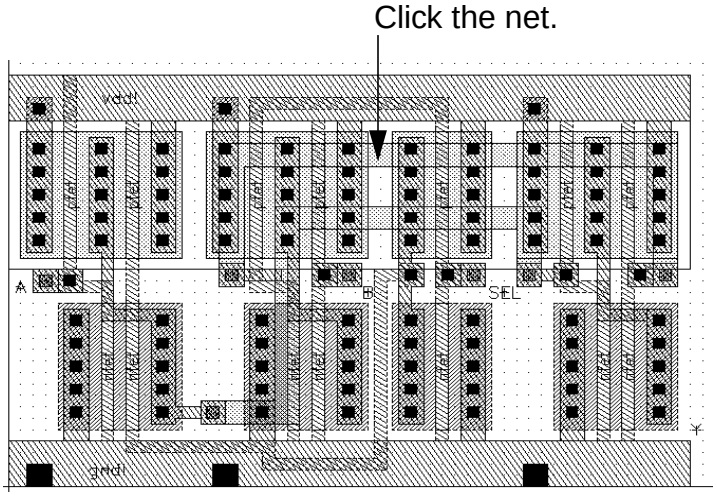
The extracted cellview window opens. The two nets are now joined.

6. In the extracted cellview window, choose *Verify – Probe*.

The Probing form opens.

7. In the Probing form, click *Add Device or Net,* and set *Probe Type* to *net only*.

8. Click left at X = 37, Y = 43 To select the net.

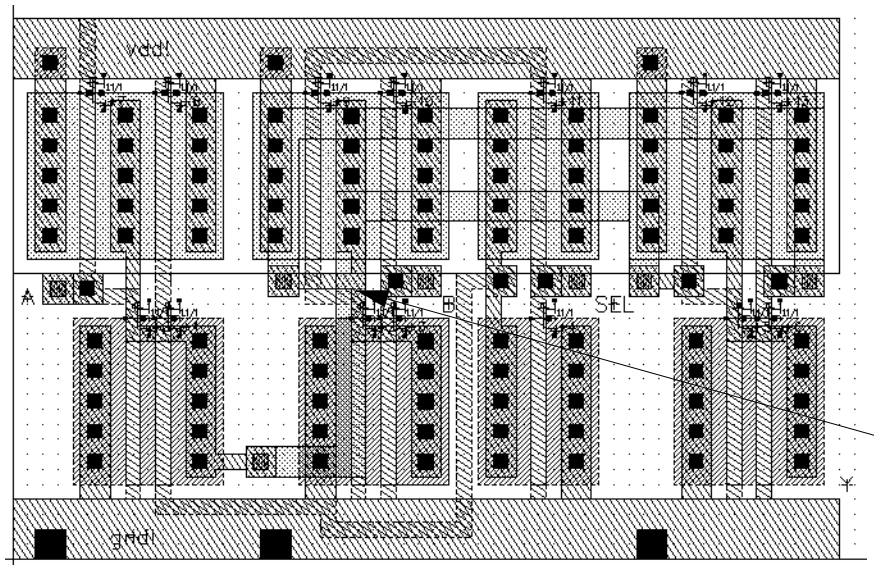


Because there are two nets at this point, a text window appears so you can choose your net from a list.

9. Click 8 in the text window to choose your net.

10. In the Probing form, click *OK*.

You can see the nets are now joined.



11. In the Probing form, click *Remove All*.

12. Click *Cancel*.

Rerunning LVS

Now you can run LVS again on the new extracted cellview.

1. In the extracted cellview window, choose *Verify – LVS* to open the LVS form.
2. In the LVS form, click *Run*.

   A form asks if you want to save the cellview.
3. Click *OK* to save the *mux2* layout.

   The LVS job proceeds, then a dialog box appears, confirming the job has been completed. This might take a few minutes.
4. Click *OK* to close the dialog box.
5. In the LVS form, click *Output*.

   A text window containing the LVS report appears. The message in the text window should read:

   ```
   The net-lists match
   ```
6. In the text window, choose *File – Close Window*.
7. In the LVS form, choose *Commands – Close Window*.
8. In the extracted cellview window, choose *Window – Close*.
9. In the layout cellview window, choose *Window – Close*.

   You have completed verifying the *mux2* layout.

Summary

In this chapter, you learned how to verify layout designs using interactive verification. Specifically, you

- Ran a DRC (Design Rule Checker)
- Viewed DRC errors
- Extracted a layout view
- Viewed extracted data
- Viewed a schematic
- Ran LVS
- Viewed LVS errors
- Cross-probed between the extracted layout and the schematic
- Ran verification programs again
- Used bindkeys:
  - Redraw [`Control-r`]
  - Zoom In [z]
  - Display Options [e]
  - Stretch [s]
  - Display Levels 0–20 [`Shift-f`]
  - Display Levels 0–0 [`Control-f`]

- Fit All [f]

- Used the icon menu for *Save*